

MY6 BLOCK DIAGRAM

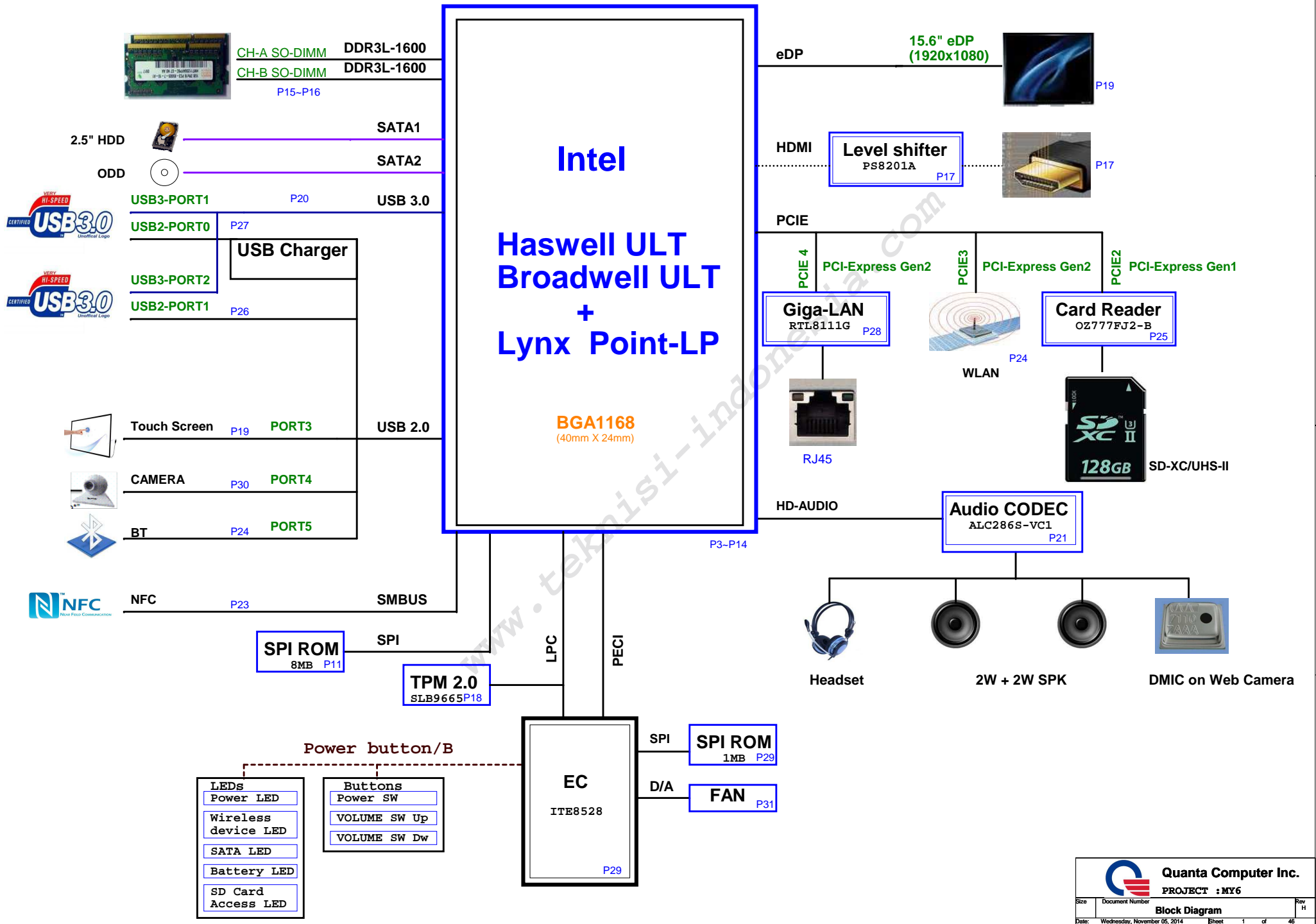


Table of Contents

PAGE	DESCRIPTION
01	Schematic Block Diagram
02	Front Page
03	HSW MCP(Display/eDp)
04	HSW MCP(Memory)
05	HSW MCP(Gnd/Daisy/Rsvd)
06	HSW MCP(CFG)
07	HSW MCP(Sideband/XDP)
08	HSW MCP(Power)
09	HSW PCH(RTC/HDA/SATA)
10	HSW PCH(PCIE/USB)
11	HSW PCH(CLK/LPC/SPI/SMB)
12	HSW PCH(GPIO/LPIO/MISC)
13	HSW PCH(Power Management)
14	HSW PCH(Power)
15	DDR3 SODIMM-0
16	DDR3 SODIMM-1
17	HDMI
18	TPM
19	Panel Control/Touch
20	HDD/ODD
21	AUDIO(ALC286S-VC1)
22	EMI
23	NFC
24	MINI PCIE(WLAN/BT)
25	Card Reader(OZ777FJ2-B)
26	USB 3.0 CONN
27	USB3.0 Conenctor/Charge
28	RTL8111G
29	EC(IT8528)
30	LED/Camera
31	FAN/NUT
32	CPU Core (ISL95813HRZ)ULT
33	POWER 3VS5&5VS5(TPS51427A)
34	Power +1.35V_SUS/DDR_VTTERM
35	Power +1.05V/+1.5V
36	Power Thermal Protection
37	Power AD IN
38	PWR Charger (OZ8682)
39	Discharger
40	Load SW
41	Clock Distribution
42	Power Sequence
43	Power Tree
44	SMBUS Address
45	RESET MAP
46	Change List

Voltage Rails

Power	Voltage	S0	S3	S4	S5	Ctl Signal
+5VPCU	5V	V	V	V	V	+5VPCU_6686 (TPS51427ARHBR)
+3VPCU	3.3V	V	V	V	V	+5VPCU_6686 (TPS51427ARHBR)
3V_LAN	3.3V	V	Note1	Note1	Note1	15V_LAN_ON
3V_WLAN	3.3V	V	Note1	Note1	Note1	15V_WLAN_ON
5V_S5	5V	V	V	V		15V_S5_ON
3V_S5	3.3V	V	V	V		15V_S5_ON
+1.35V_SUS	1.35V	V	V			S3_ON
+0.675V_DDR_VTT	0.675V	V	V			S3_ON
DDR_VTTREF	0.675V	V	V			S3_ON
+1.05V	1.05V	V				S0_ON_2
1.5V_S0	1.5V	V				S0_ON_1
5V_S3	5V	V	V			15V_S3_ON
5V_S0	5V	V				15V_S0_ON1
3V_S0	3.3V	V				15V_S0_ON1
+VCC_CORE	BY VID	V				VRON

Note1 : Deoend on WOL

F/W List

	Location	Update method
BIOS/ME	U2	Flash tool in Windows
EC	U25	Flash tool in Windows

Resister tolerance:
F :+/- 1%, (example:69.8K/F_4)
others are +/- 5%, (example:69.8K_4)

Capacitor tolerance:
X7R: +/- 10%
X5R: +/- 10%
Y5V: +80%~-20%
others are +/- 5%

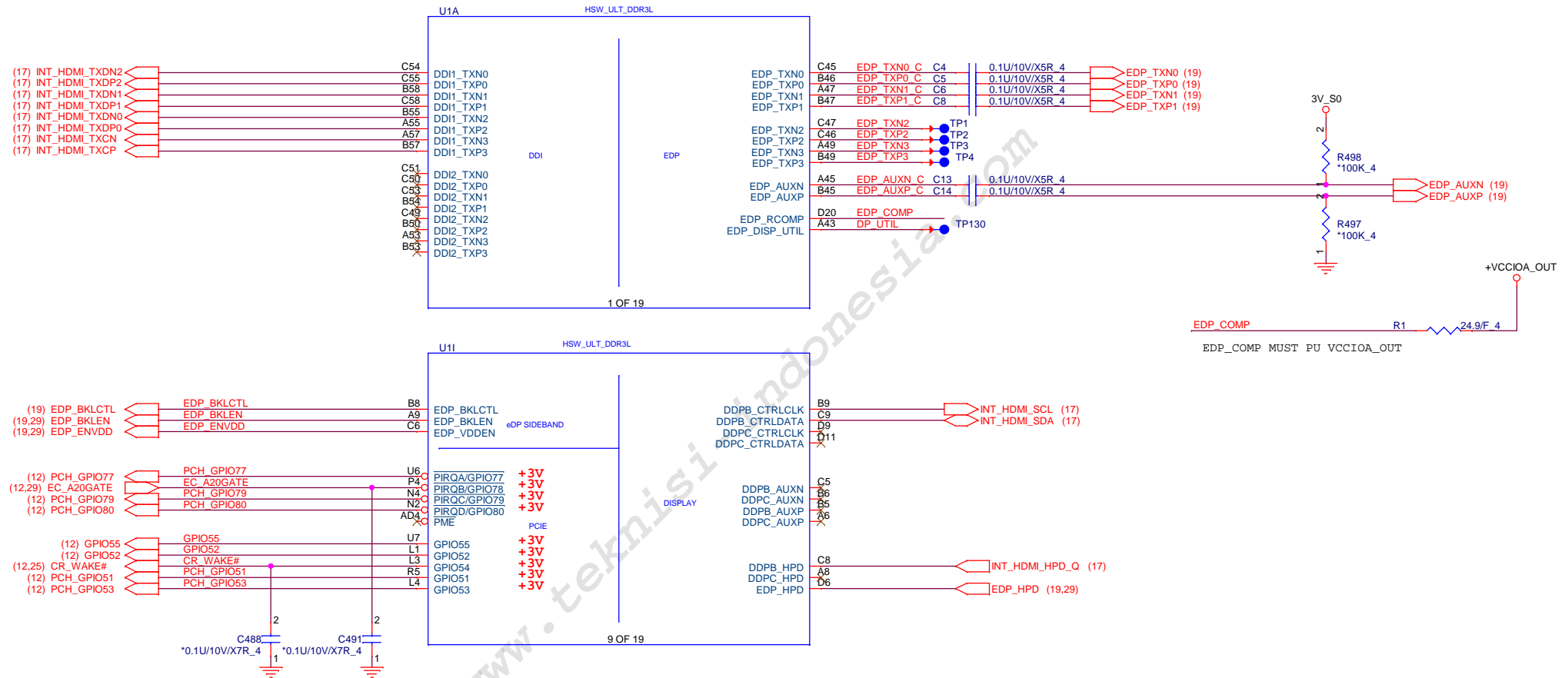
PCB STACK UP

6L

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

02

Haswell ULT (DISPLAY)



1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.



Quanta Computer Inc.

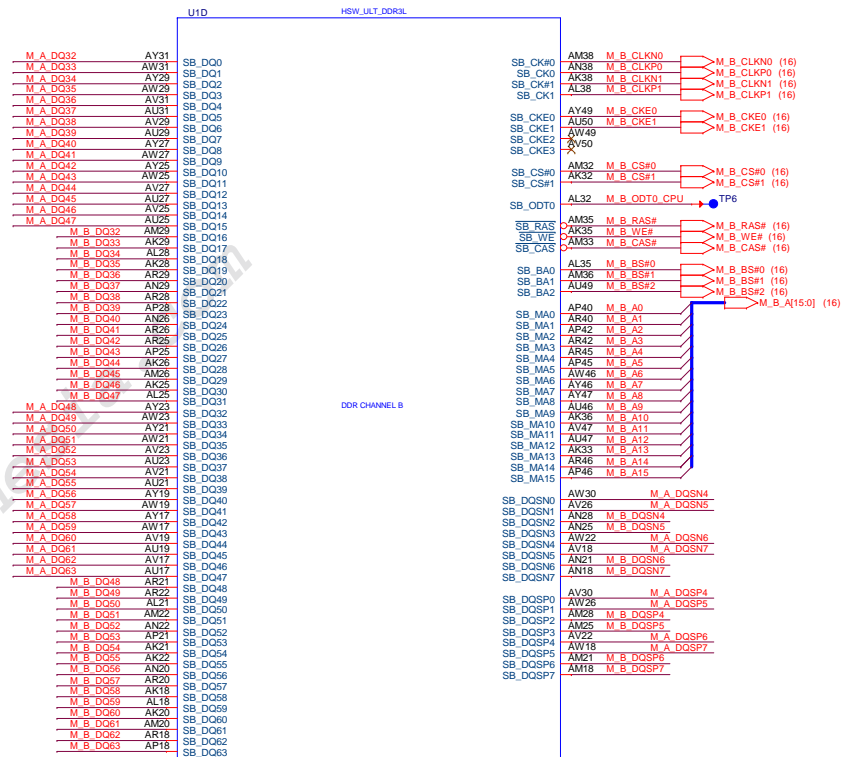
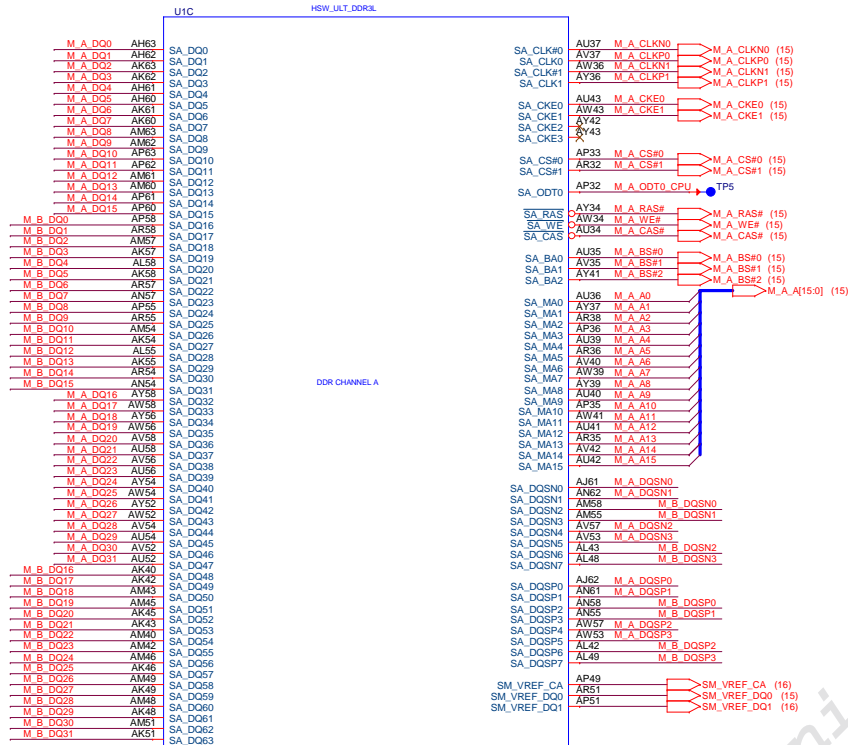
PROJECT : MY6

Size	Document Number	Rev
	HSW MCP(Display/eDP)	H


Date: Wednesday, November 05, 2014 Sheet 3 of 46

Haswell ULT (DDR3L Interleaved PIN)

(15) M_A_DQ[63:0]  M_A_DQSN[7:0] (15)
 (16) M_B_DQ[63:0]  M_A_DQSP[7:0] (15)
 M_B_DQSN[7:0] (16)
 M_B_DQSP[7:0] (16)



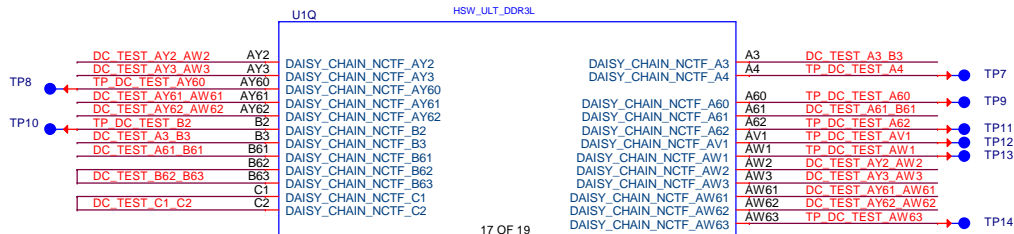
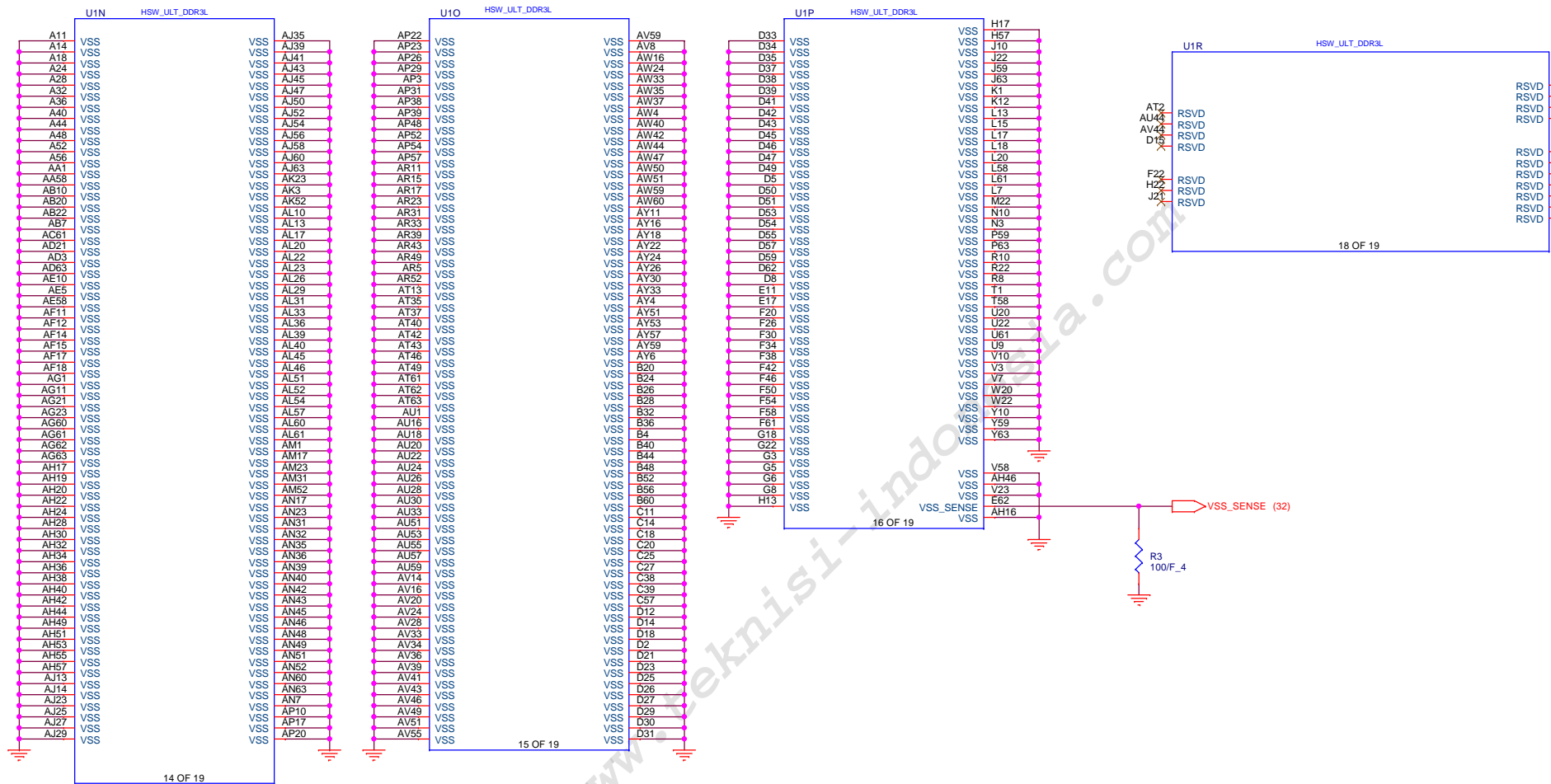
1. Level 1 Environment-related Substances should Never be Used.
 2. Recycled Resin and Coated Wire should be procured from Green Partners.


Quanta Computer Inc.
PROJECT : MY6

Size	Document Number	Rev
	HSW MCP(Memory)	H
Date: Wednesday, November 05, 2014	Sheet 4 of 46	

Haswell ULT (GND)

05



1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

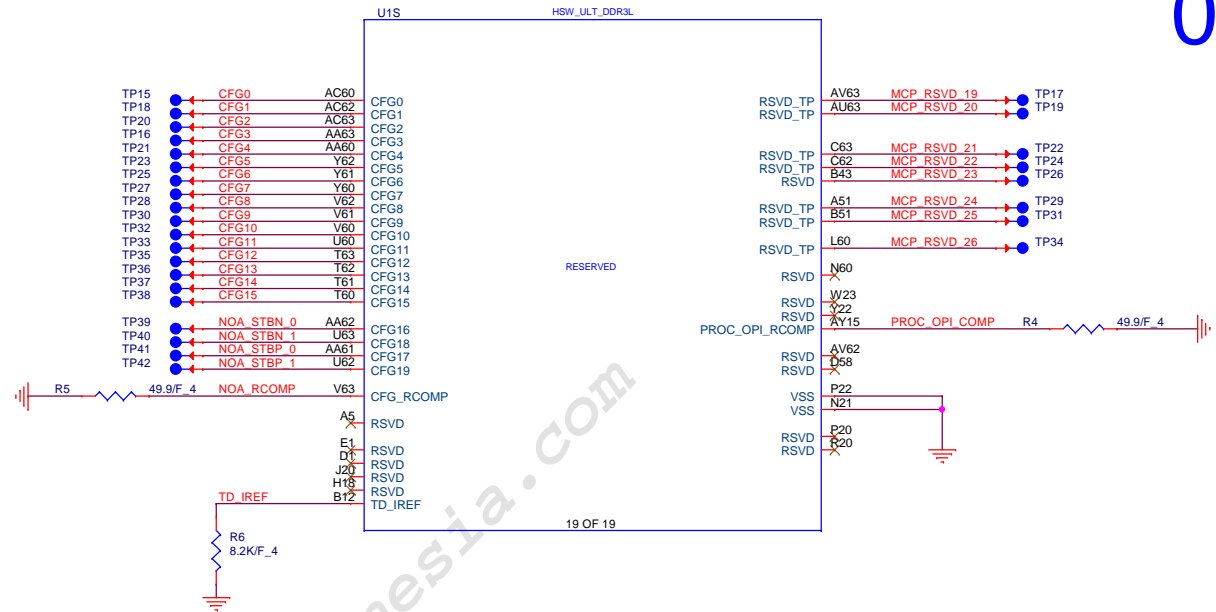


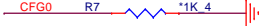
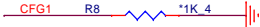
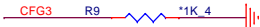
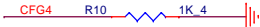



Quanta Computer Inc.

PROJECT : MY6

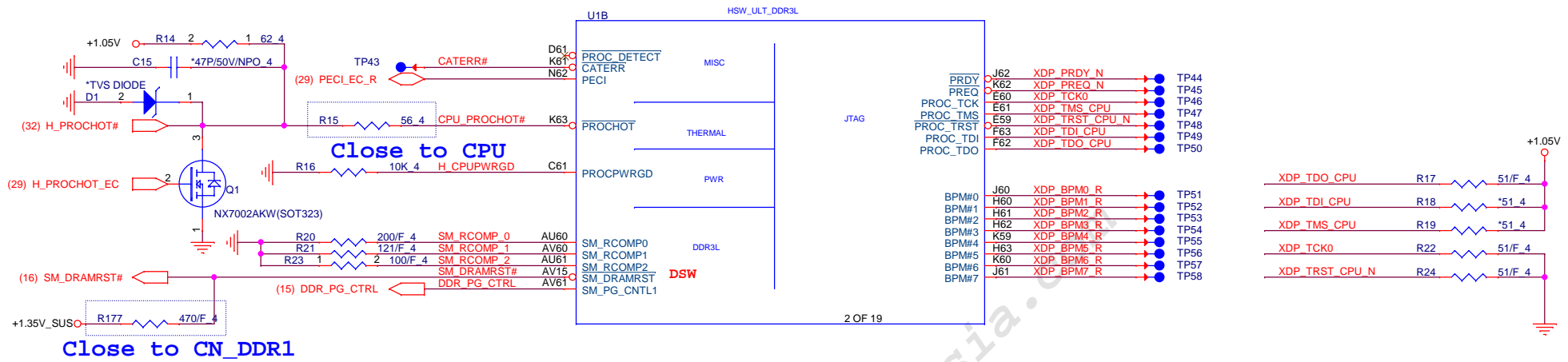
HSW MCP(GND/RSVD)

Size	Document Number	Rev
		H
Date:	Wednesday, November 05, 2014	Sheet 5 of 46



	1	0	
CFG[2:0] Reserved configuration lane.	(DEFAULT) NORMAL OPERATION; NO STALL (DEFAULT) NORMAL OPERATION	STALL PCH-LESS MODE	 
CFG[3] MSR Privacy Bit Feature	(DEFAULT) Debug Capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting	IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden	
CFG[4] DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG[19:5] Reserved configuration lanes.	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	

- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners.



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



Quanta Computer Inc.

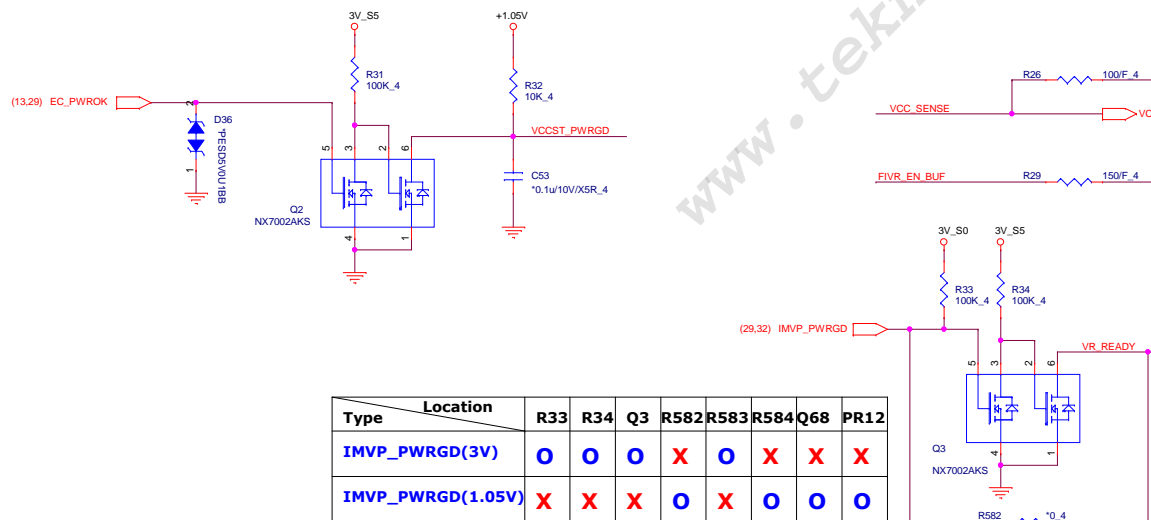
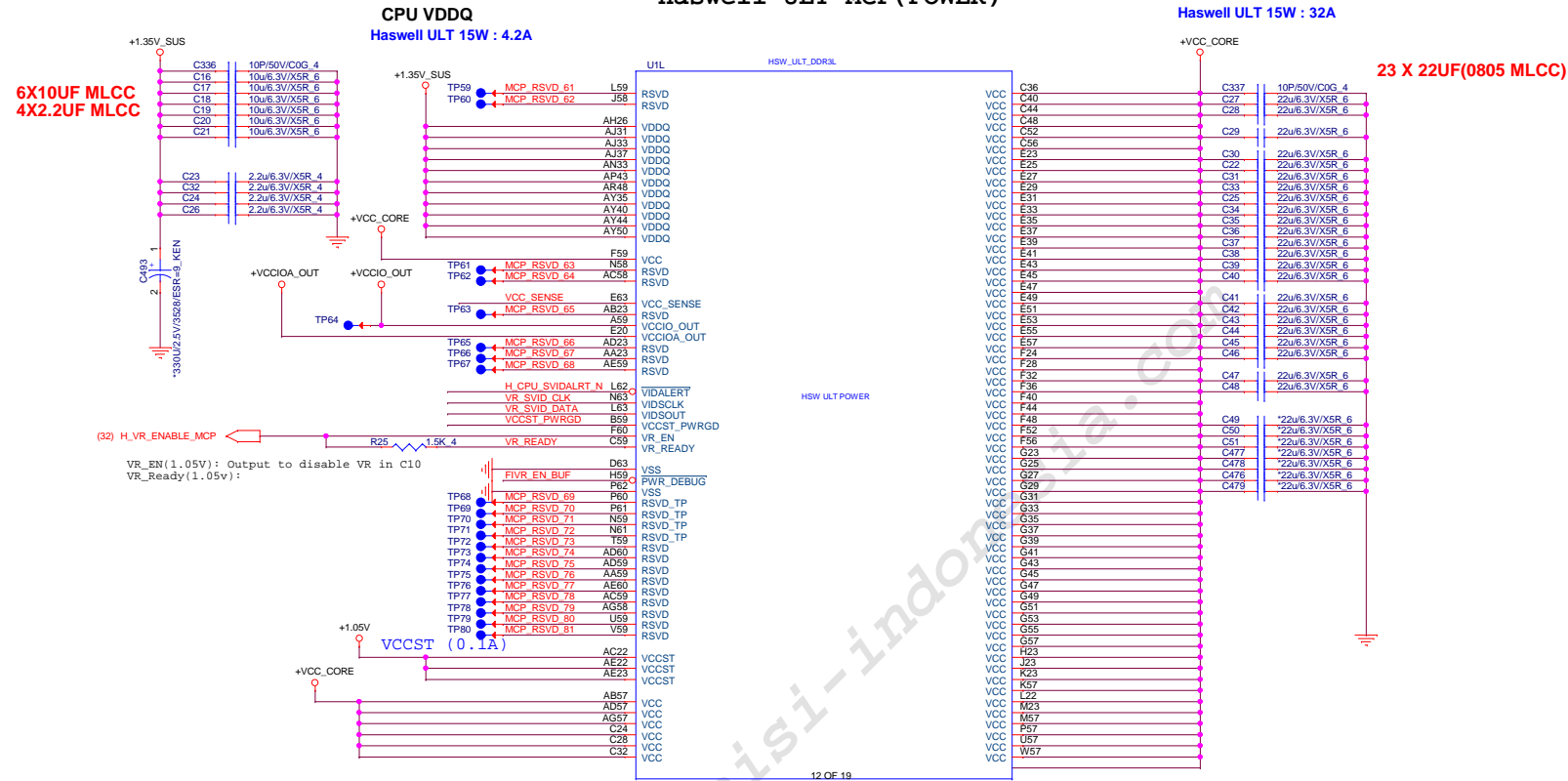
PROJECT : MY6

Size	Document Number	Rev
	HSW MCP(Sideband)	H
Date:	Wednesday, November 05, 2014	Sheet 7 of 46

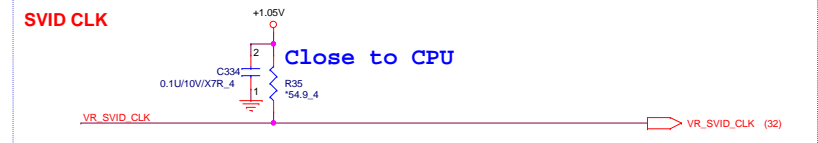
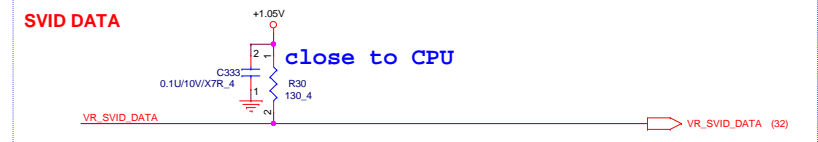
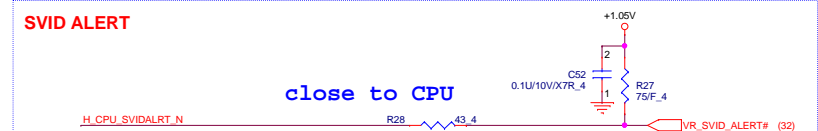
```
Haswell ULT MCP(POWER)
```

CPU VCC

Haswell ULT 15W : 32A



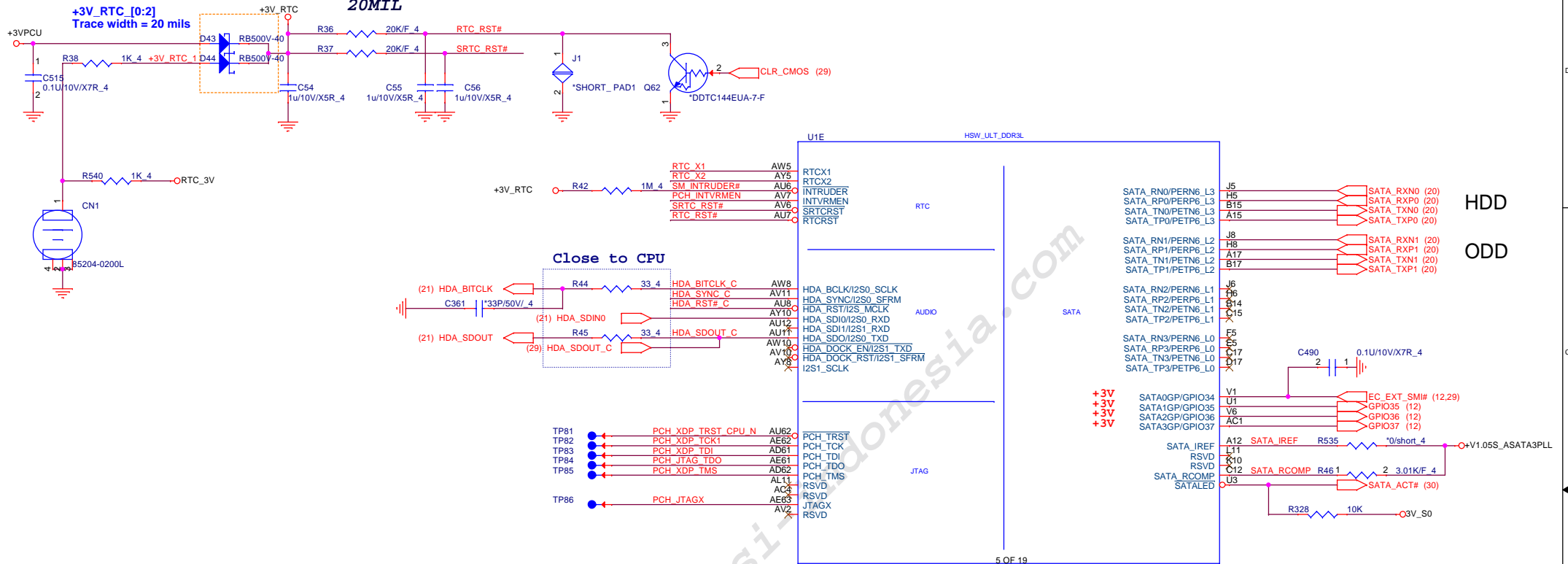
Type \ Location	R33	R34	Q3	R582	R583	R584	Q68	PR1
IMVP_PWRGD(3V)	0	0	0	X	0	X	X	X
IMVP_PWRGD(1.05V)	X	X	X	0	X	0	0	0



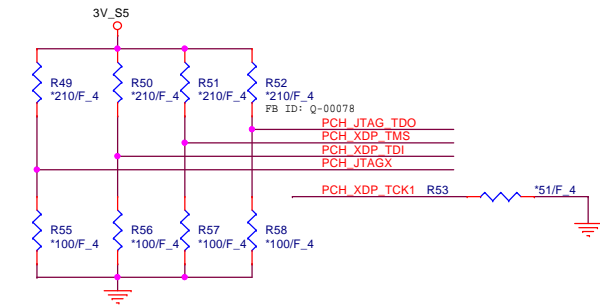
- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners.

ES2-22

20MIL

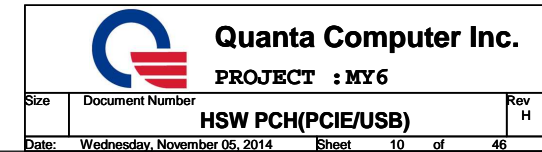


PCH JTAG Debug (CLG)



Close to CPU



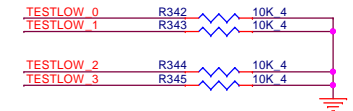
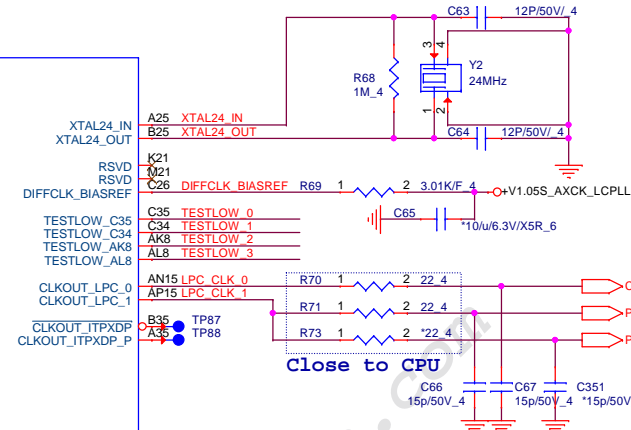
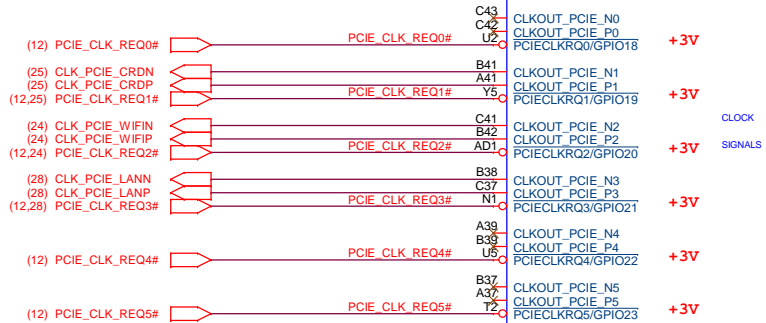


Haswell ULT (CLK)

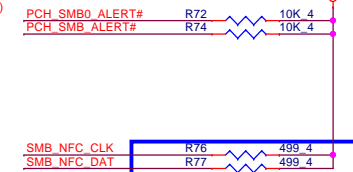
Card Reader

WiFi/BT

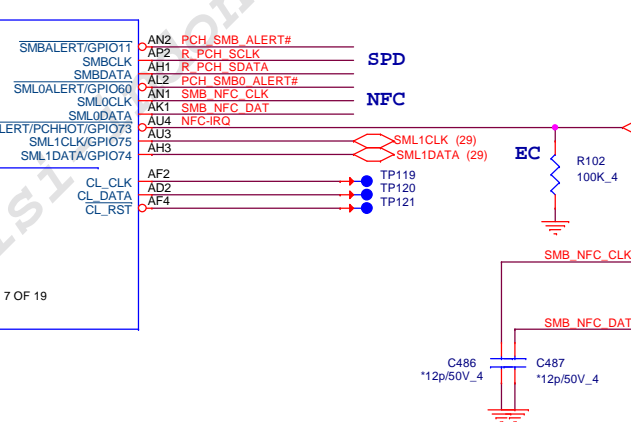
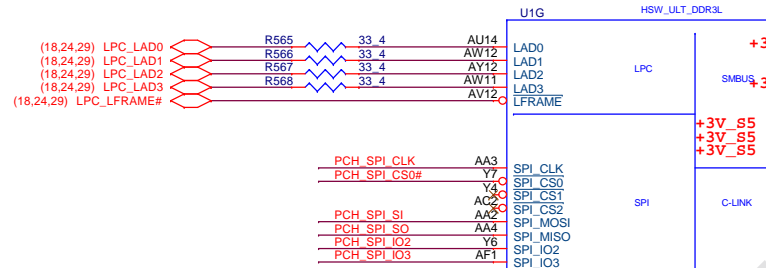
LAN



Do not short the testlow pins together.

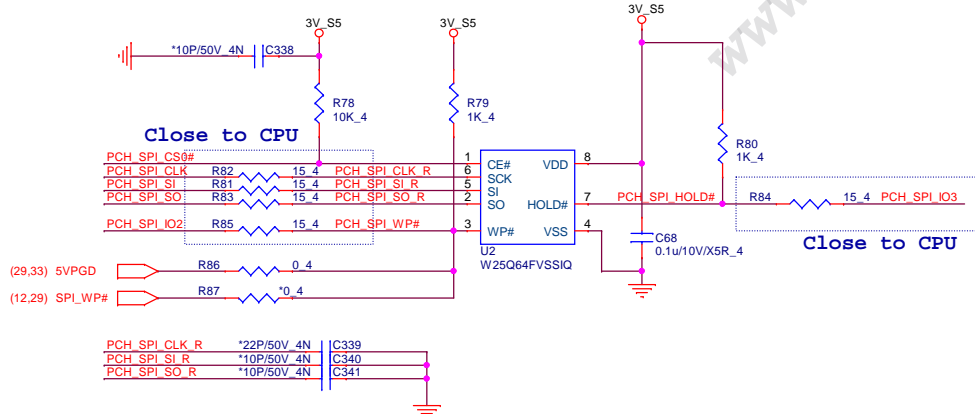
Normal Mode -> 2.2K ohm
Fast Mode -> 499 ohm

Haswell ULT (LPC/SPI/SMB/CLINK)

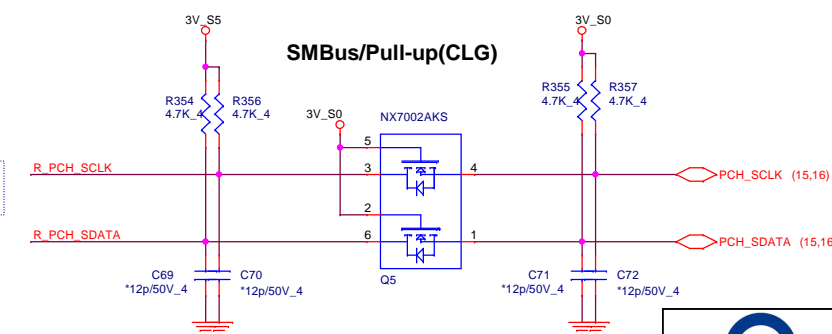


Close to CON7

SPI FLASH



SMBus/Pull-up(CLG)



Quanta Computer Inc.
PROJECT : MY6

Size	Document Number	Rev
	HSW PCH(CLK/LPC/SPI/SMB)	H
Date:	Wednesday, November 05, 2014	Sheet 11 of 46

1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

Hasswell ULT(GPIO,LPIO,MISC)

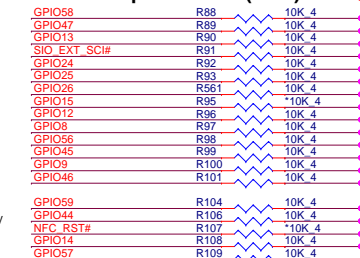
GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

GPIO27 Deep Sx



GPIO Pull-up/Pull-down(CLG)

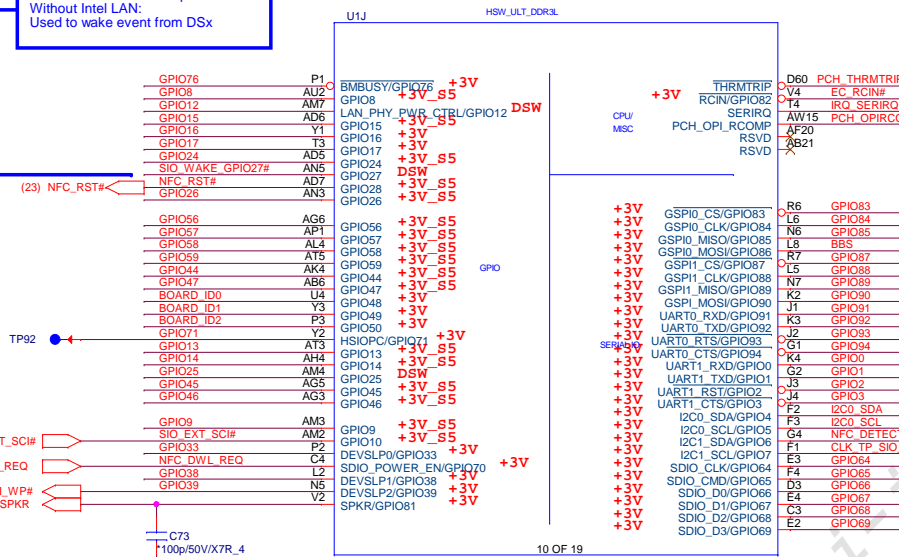
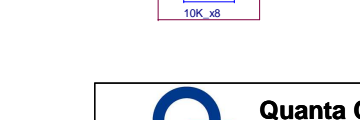
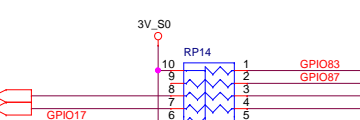
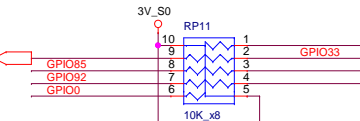
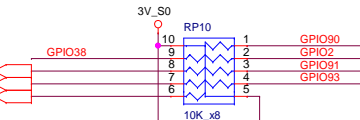
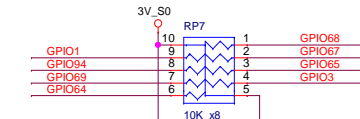


Internal PD(BIOS strap)

GPIO86 (BBS)	
PU	LPC
PD	SPI (Default IPD)

+V3.3S_1.8S_LPSS_SDIO Internal PD

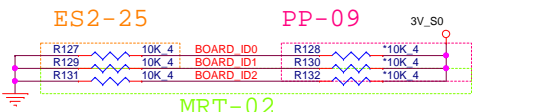
GPIO66	
R119	ENABLE
R119_NC	DISABLE(Default)



No Reboot Strap(GPIO81)	
NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

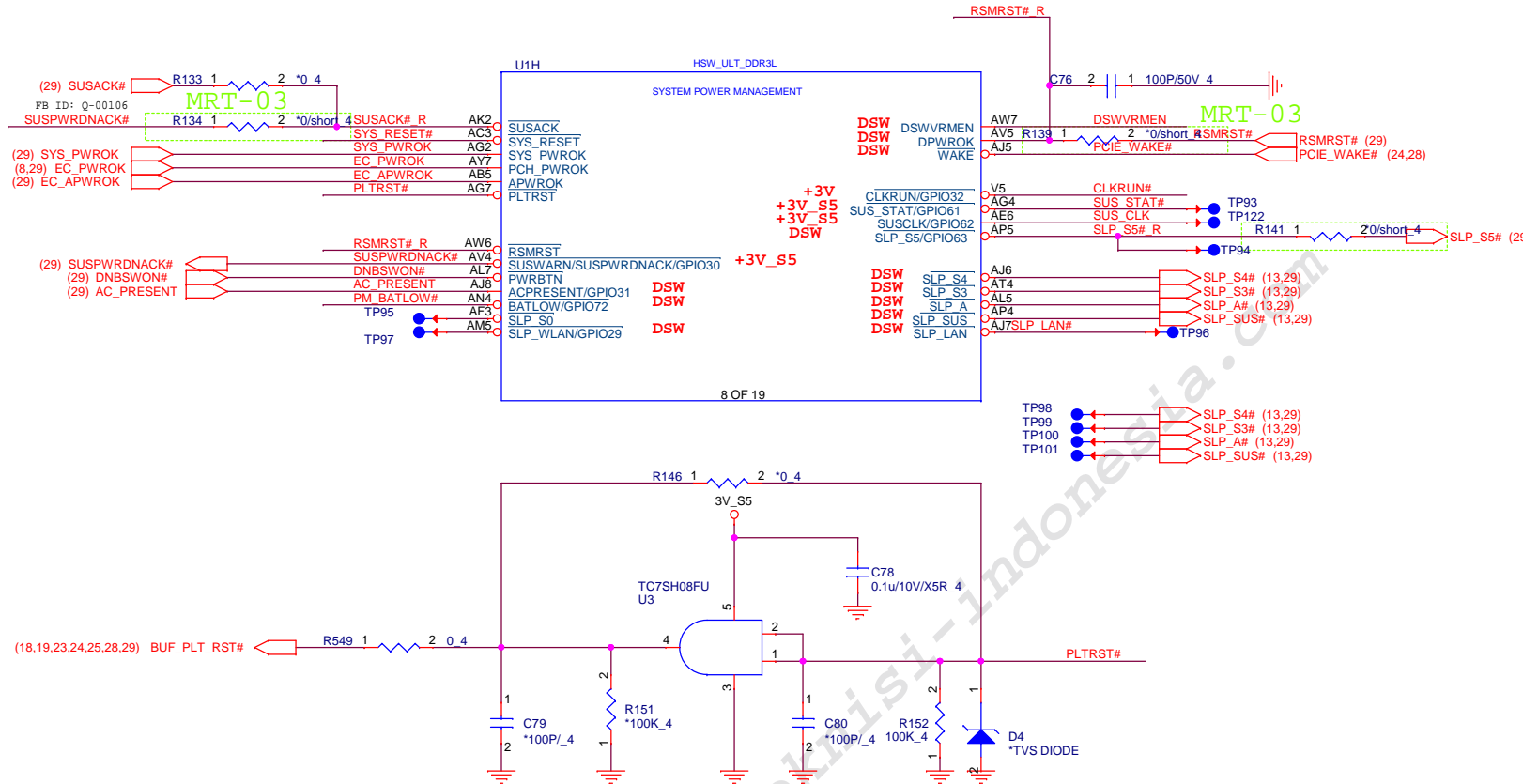
	BOARD_ID0	BOARD_ID1	BOARD_ID2
ES1	1	1	1
ES2	0	1	1
PP	0	0	1
MRT	0	0	0



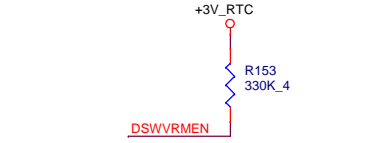
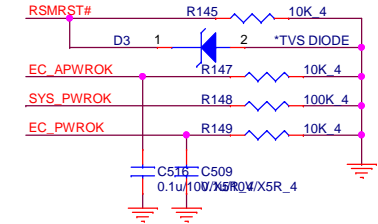
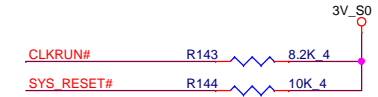
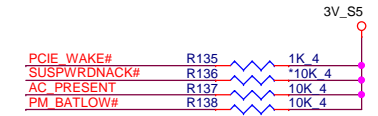
MRT-02

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Haswell ULT (SYSTEM POWER MANAGEMENT)



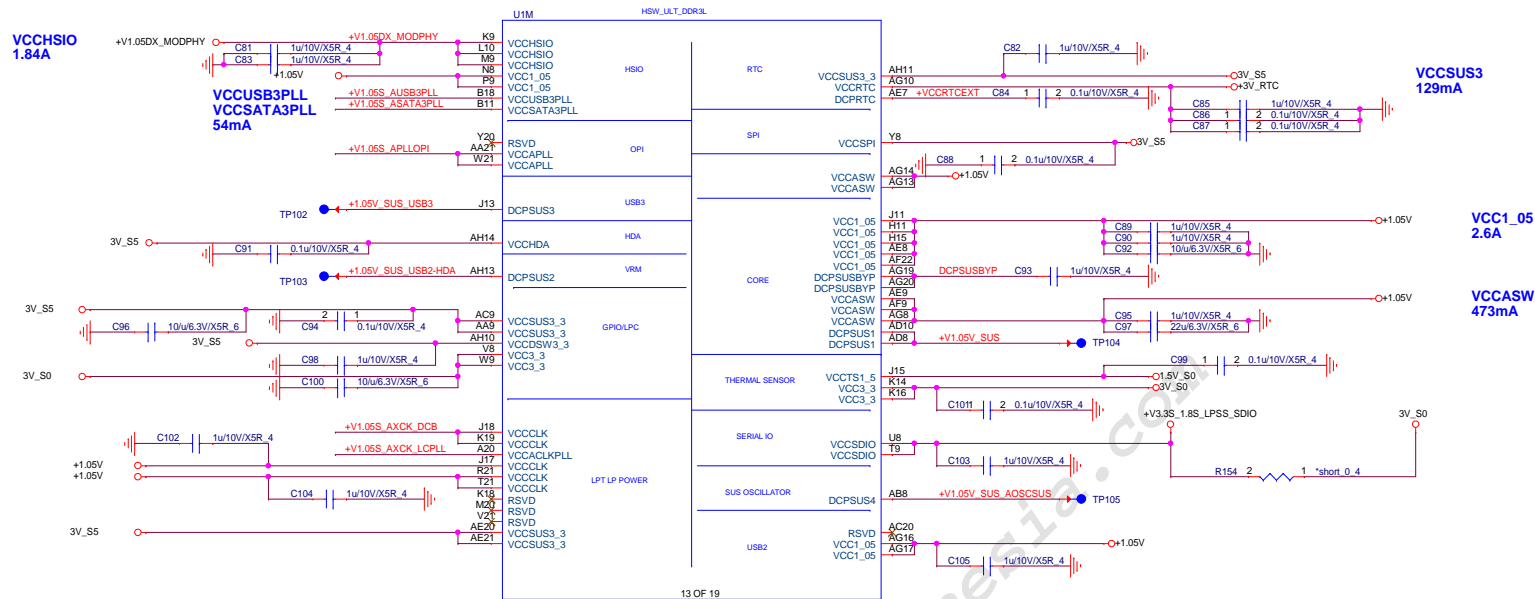
PCH Pull-high/low(CLG) 13



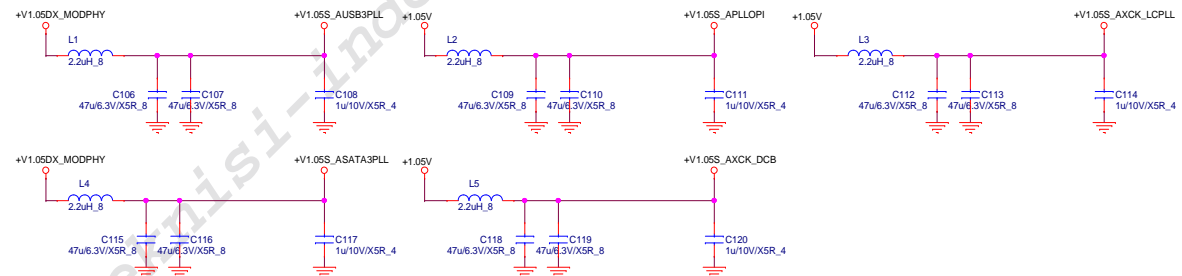
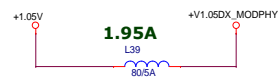
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Haswell ULT PCH(Power)



+V1.05DX_MODPHY



1. Level 1 Environment-related Substances Should Never be Used.
 2. Recycled Resin and Coated Wire should be procured from Green Partners.

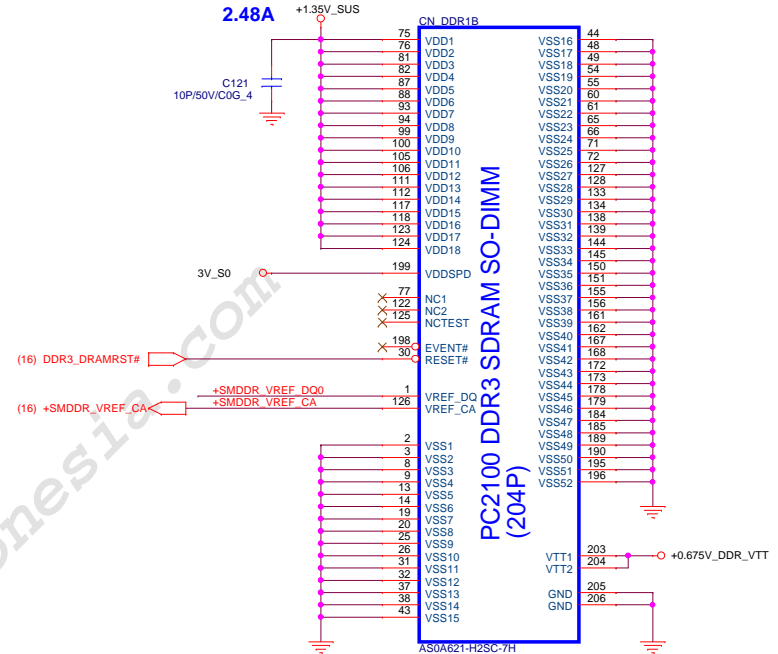


Quanta Computer Inc.

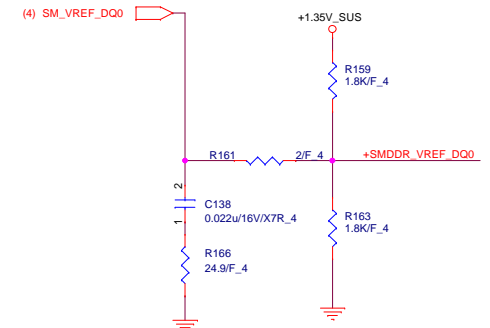
PROJECT : MY6

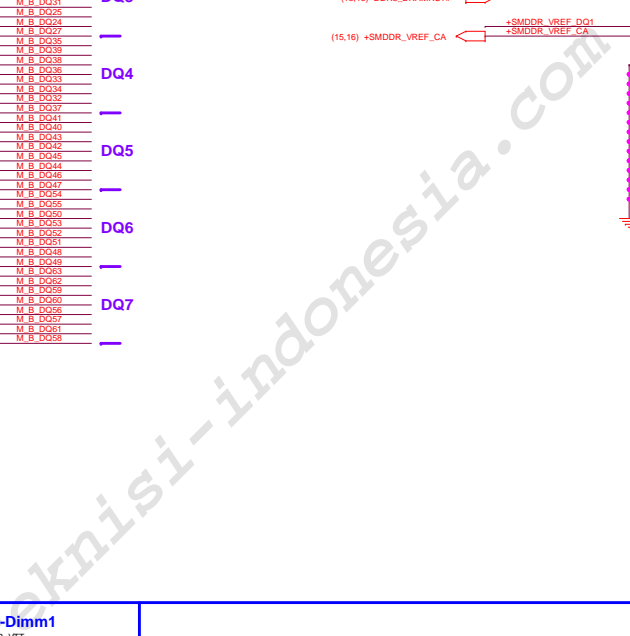
Size	Document Number	Rev
	HSW PCH(Power)	H
Date:	Wednesday, November 05, 2014	Sheet 14 of 46

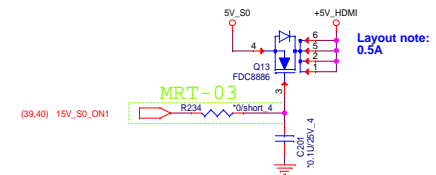
15

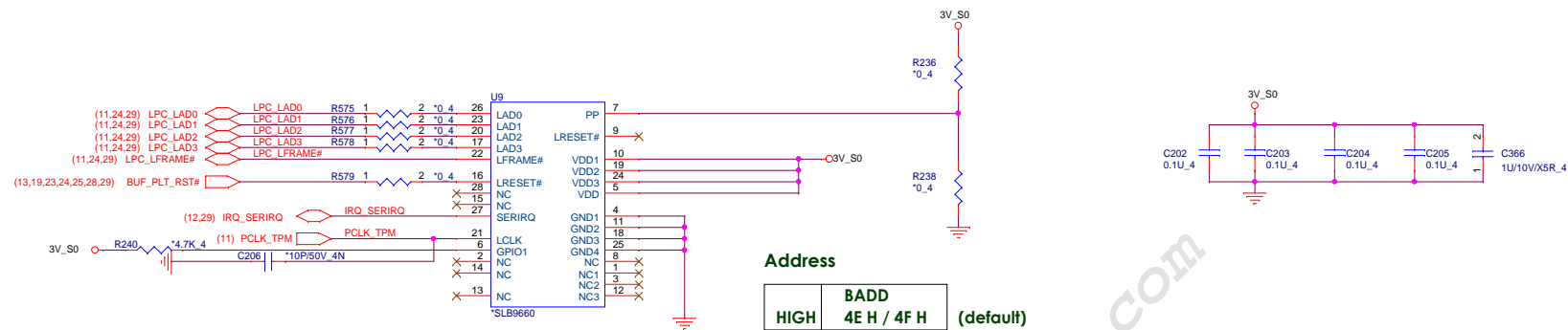


VREF DQ0 M1/M3 Solution





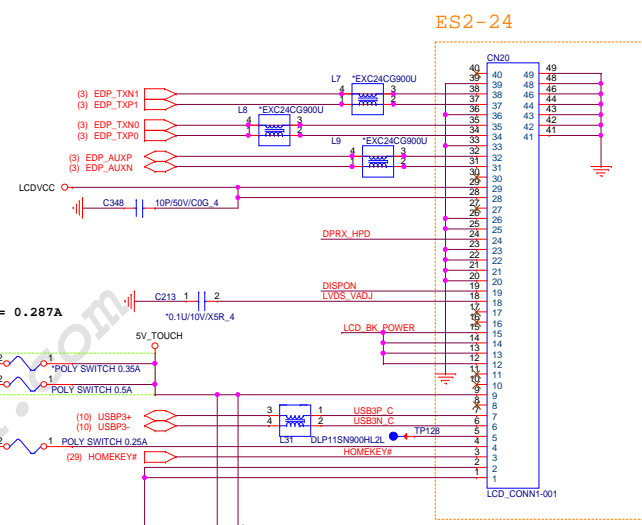
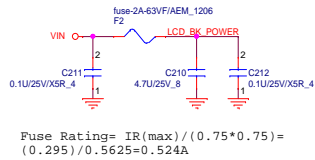
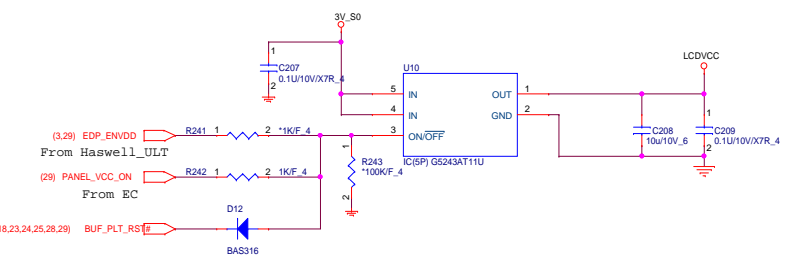




U9 TPM Support CFG	
SLB9660	TPM 1.2 (AL009660K00)
SLB9665	TPM 2.0 (AL009665K01)

LCD POWER SWITCH

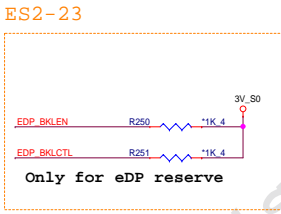
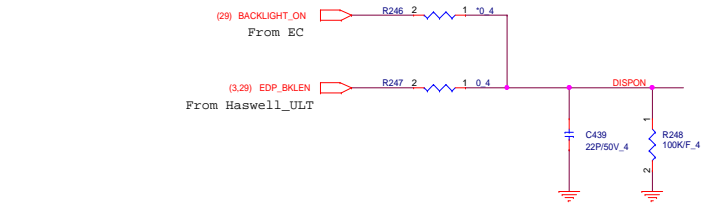
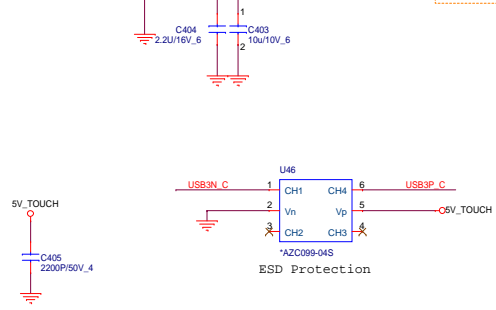
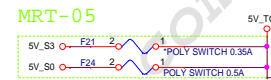
LCD Panel Module



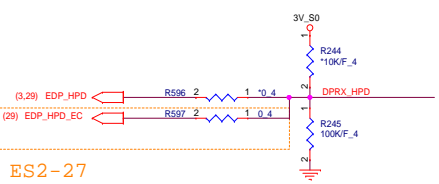
PANEL BACKLIGHT CONTROL

Touch

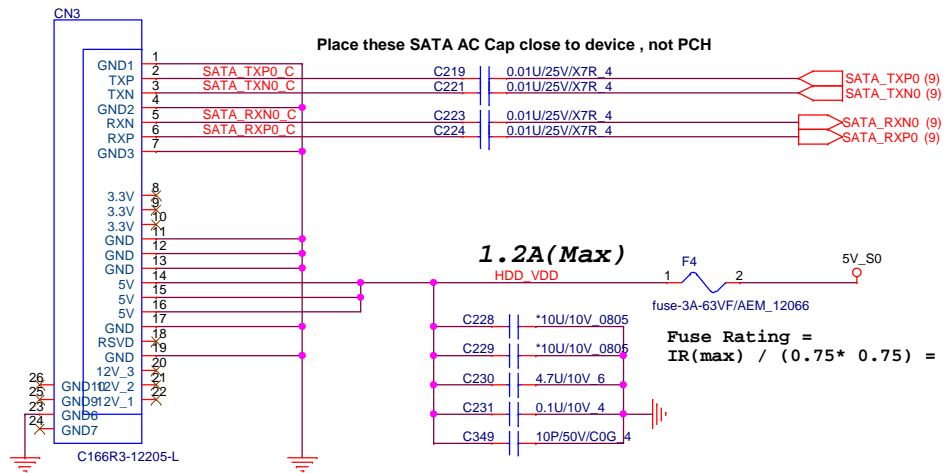
Fuse Rating = $IR(max) / (0.75 * 0.75) = 0.15A / 0.5625 = 0.287A$



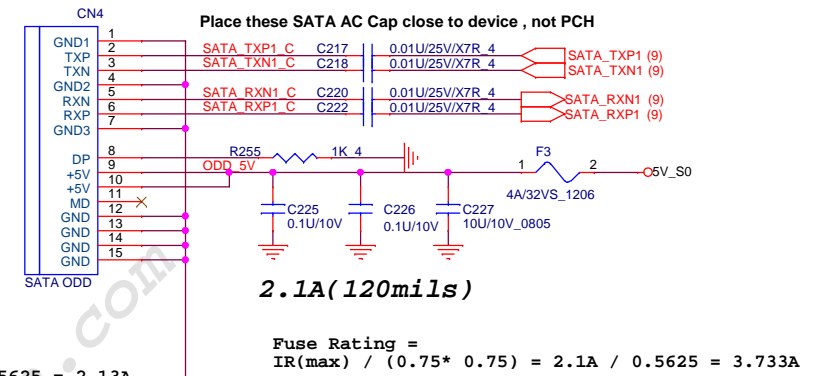
Brightness Adjust PWM CONTROL



2.5" SATA HDD



SATA ODD

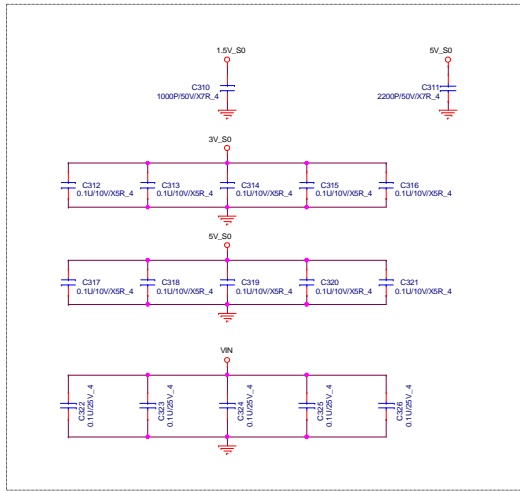


Quanta Computer Inc.

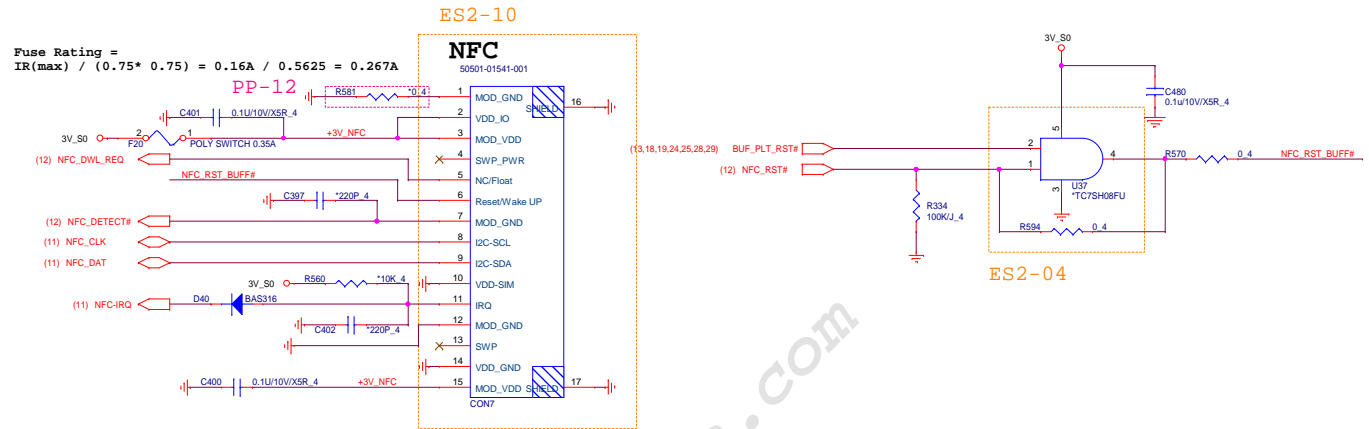
PROJECT : MY6

Size	Document Number	Rev
	HDD/ODD	H

Date: Wednesday, November 05, 2014 Sheet 20 of 46

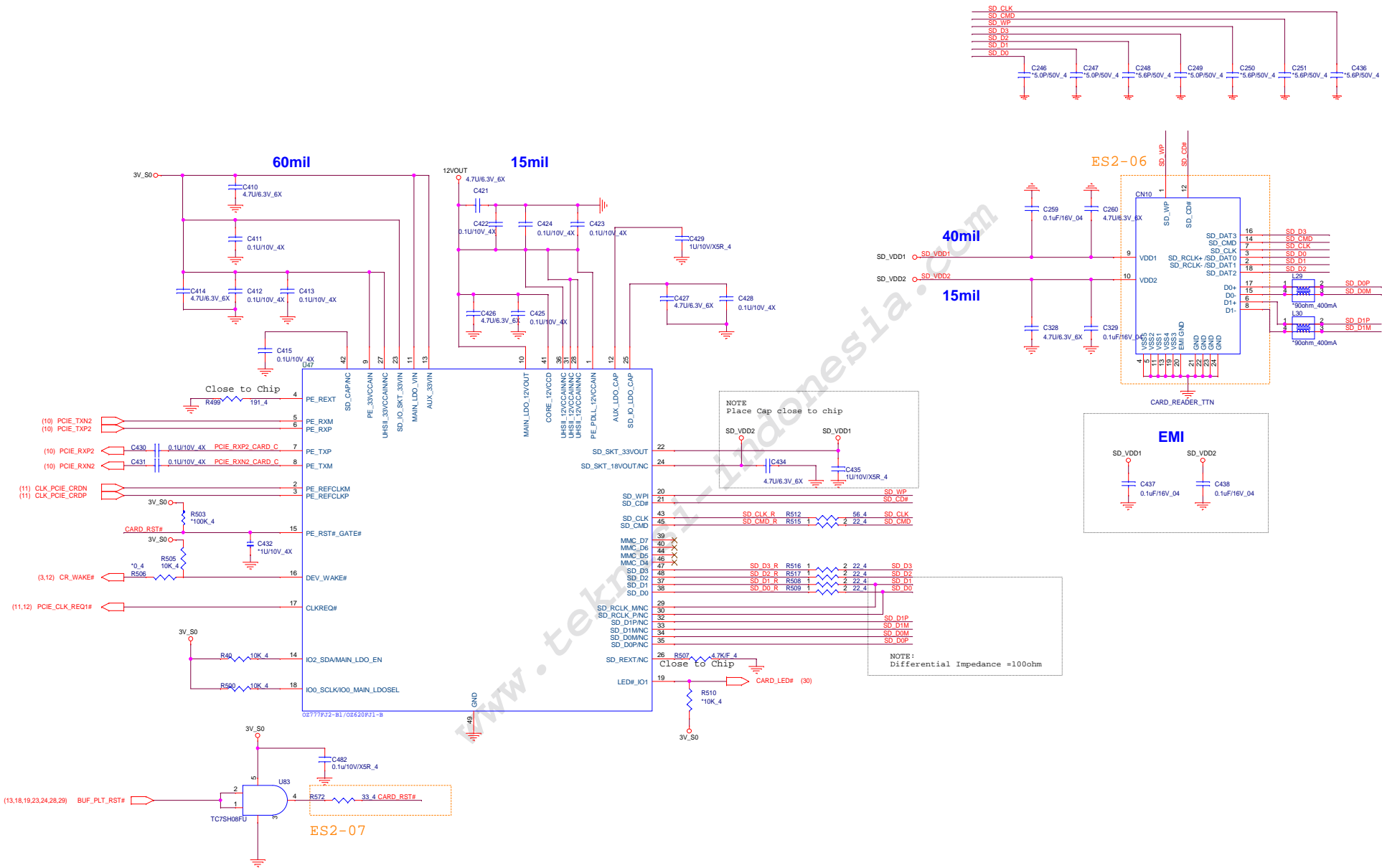


www.teknisi-indonesia.com



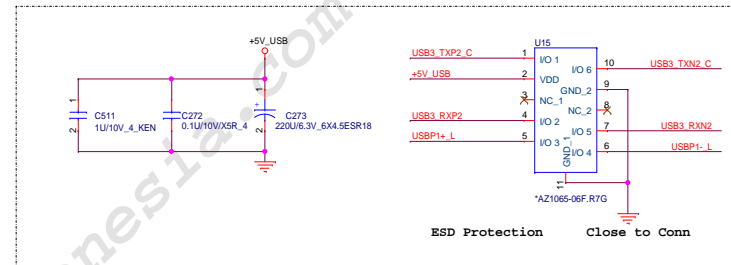
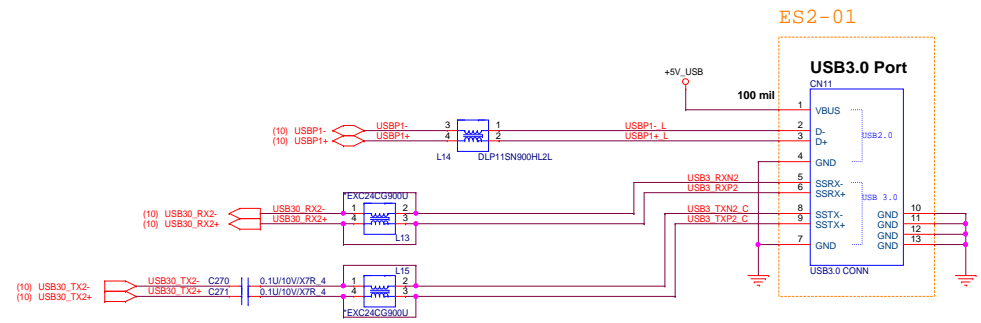
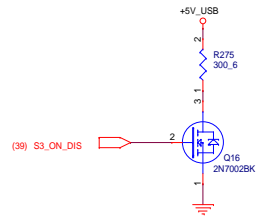
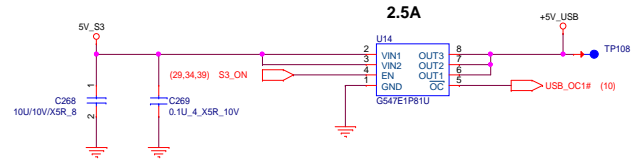


CARD READER (OZ777FJ2-B)

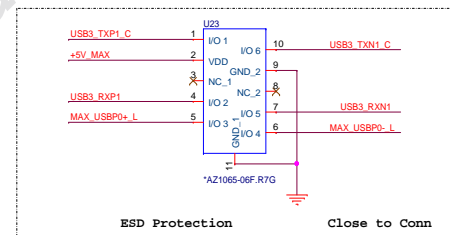
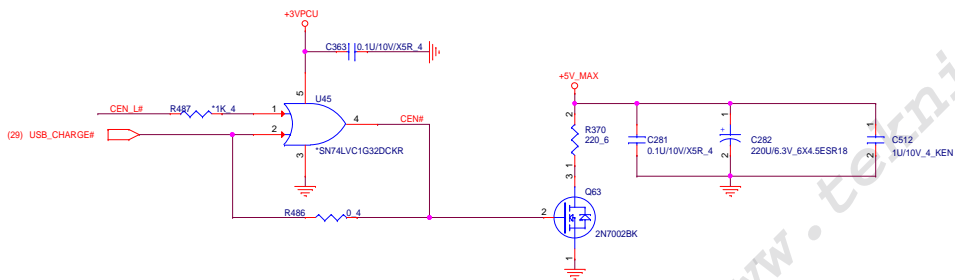
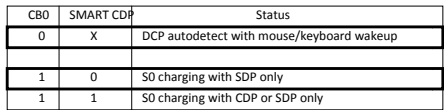


USB2.0/3.0 COMBO

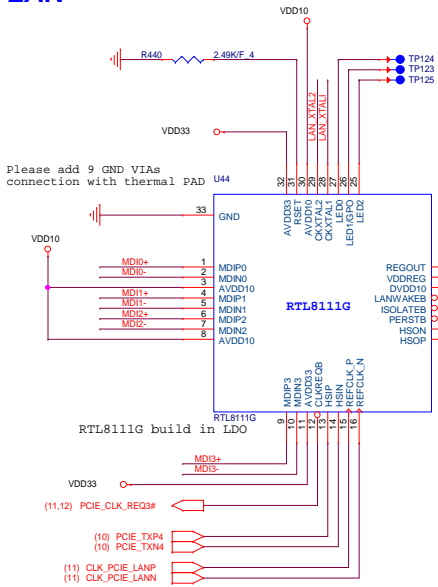
26



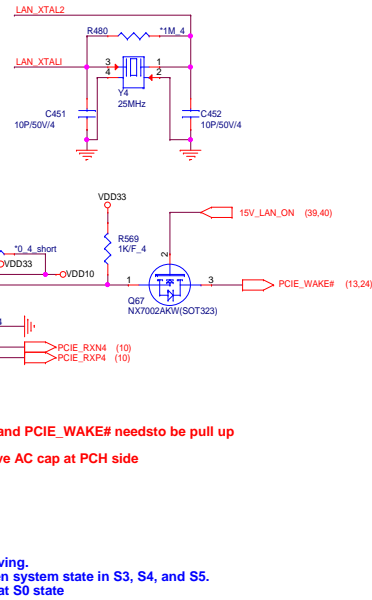
27



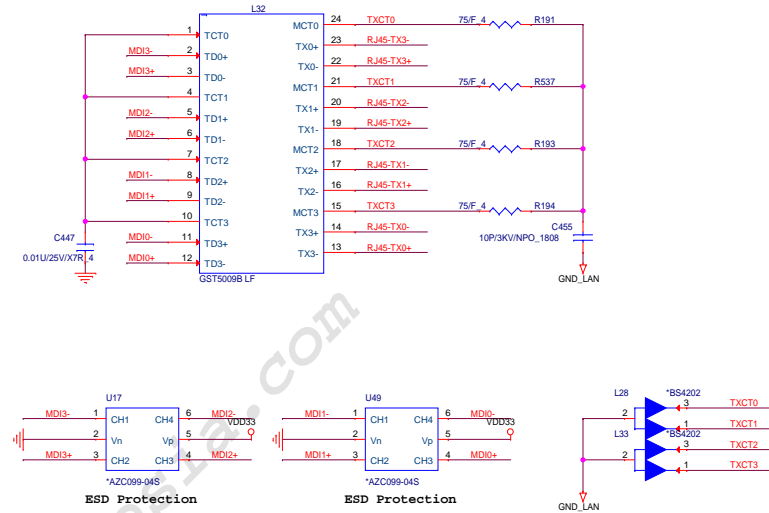
LAN



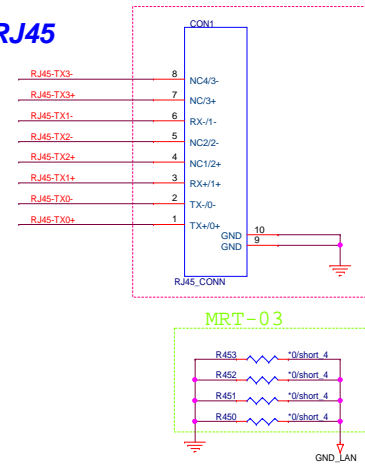
X'tal 25MHz



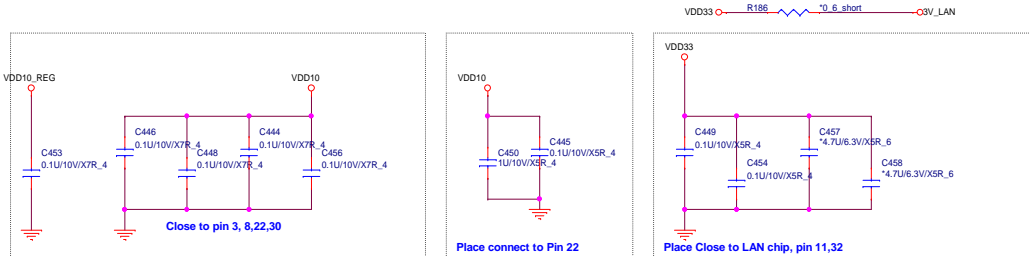
10/100/1000 Transformer

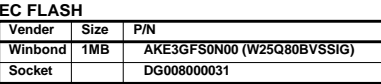


RJ45

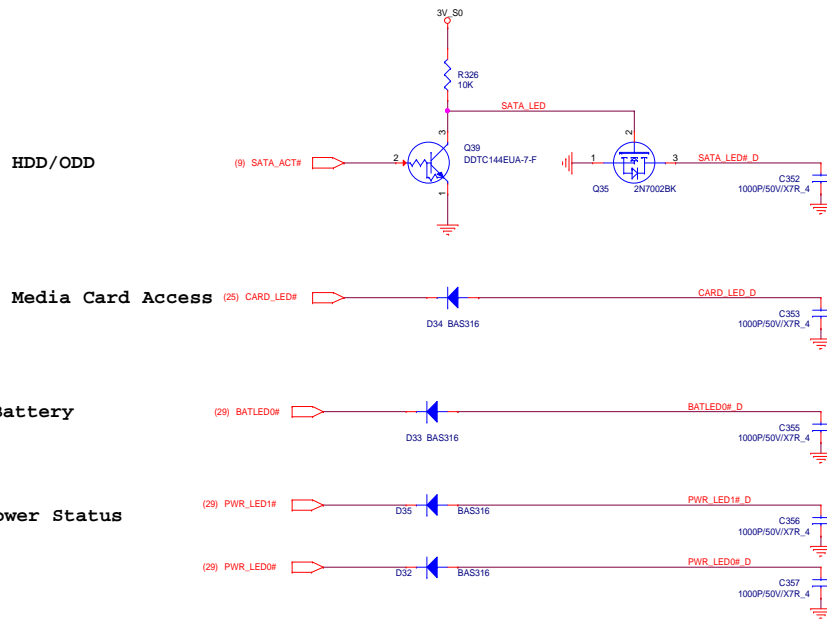


LAN Power

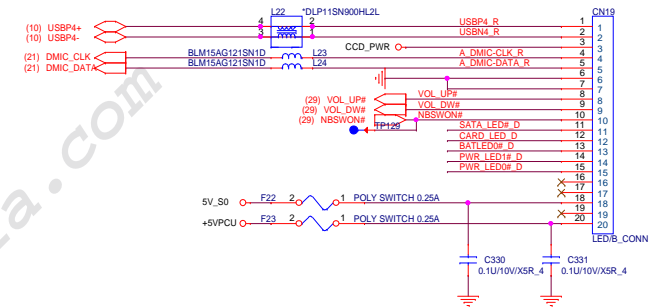
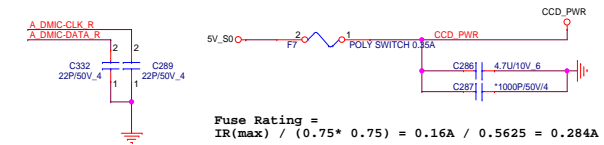


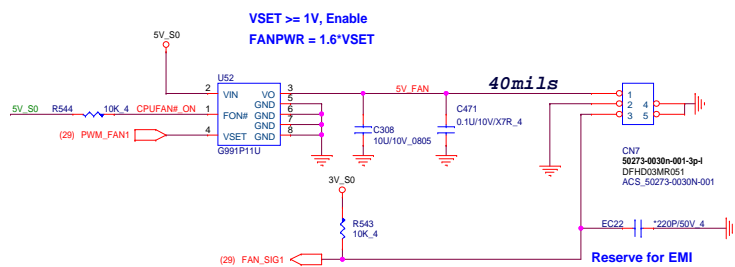


LED

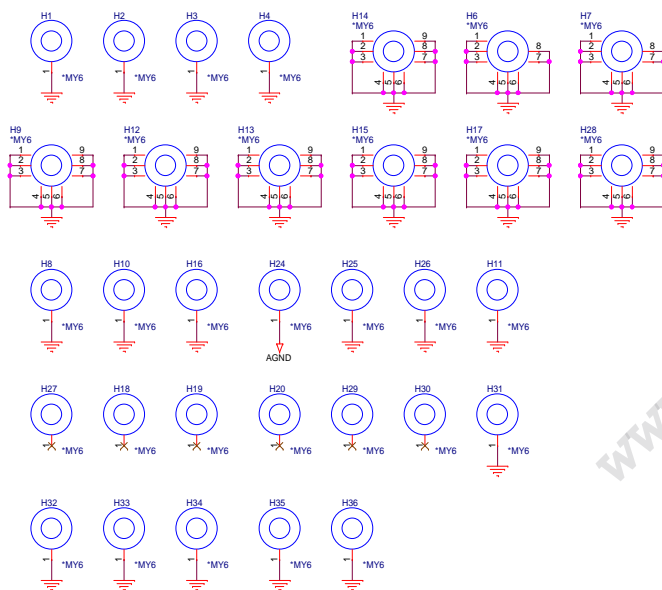


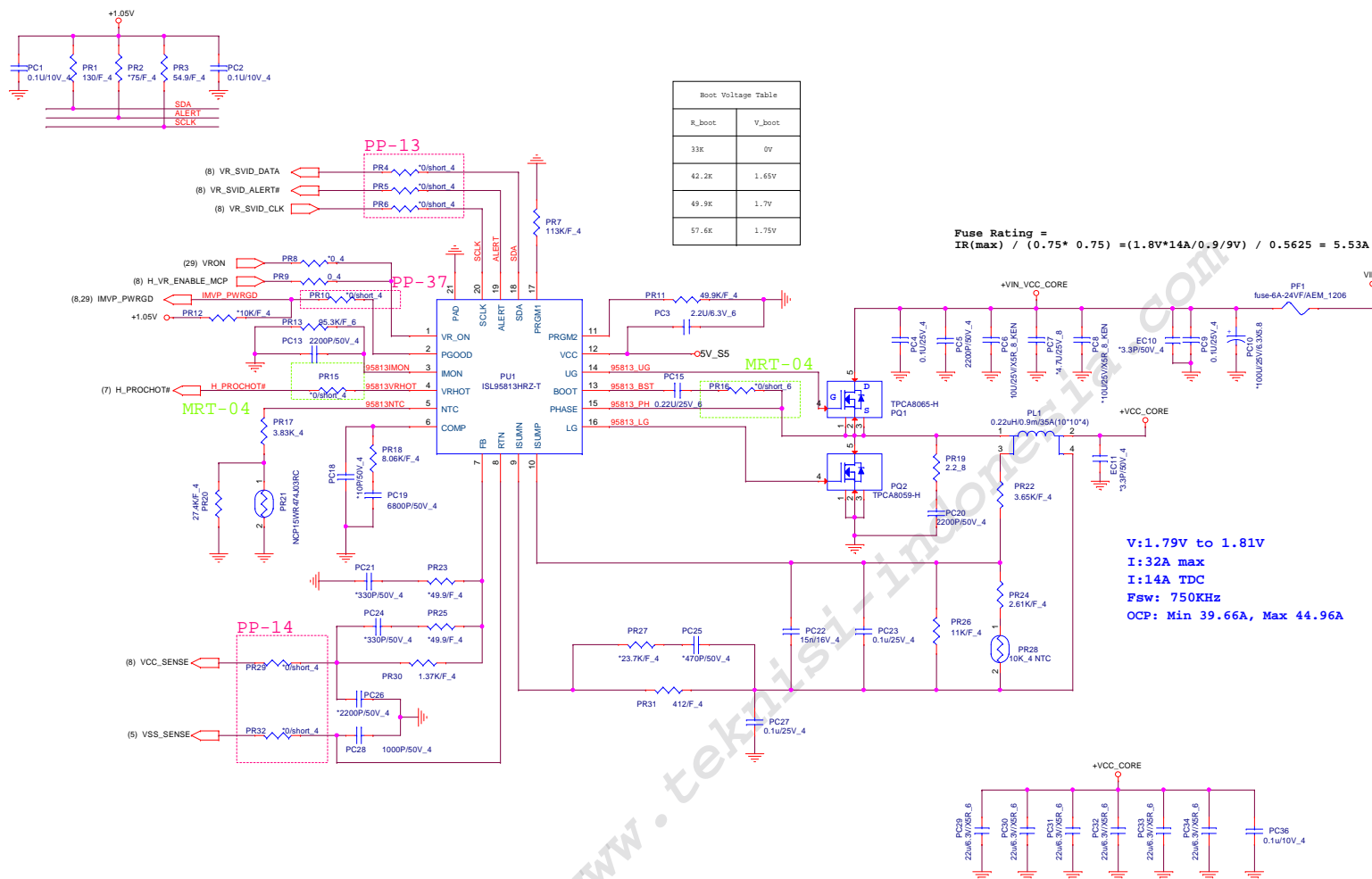
Camera



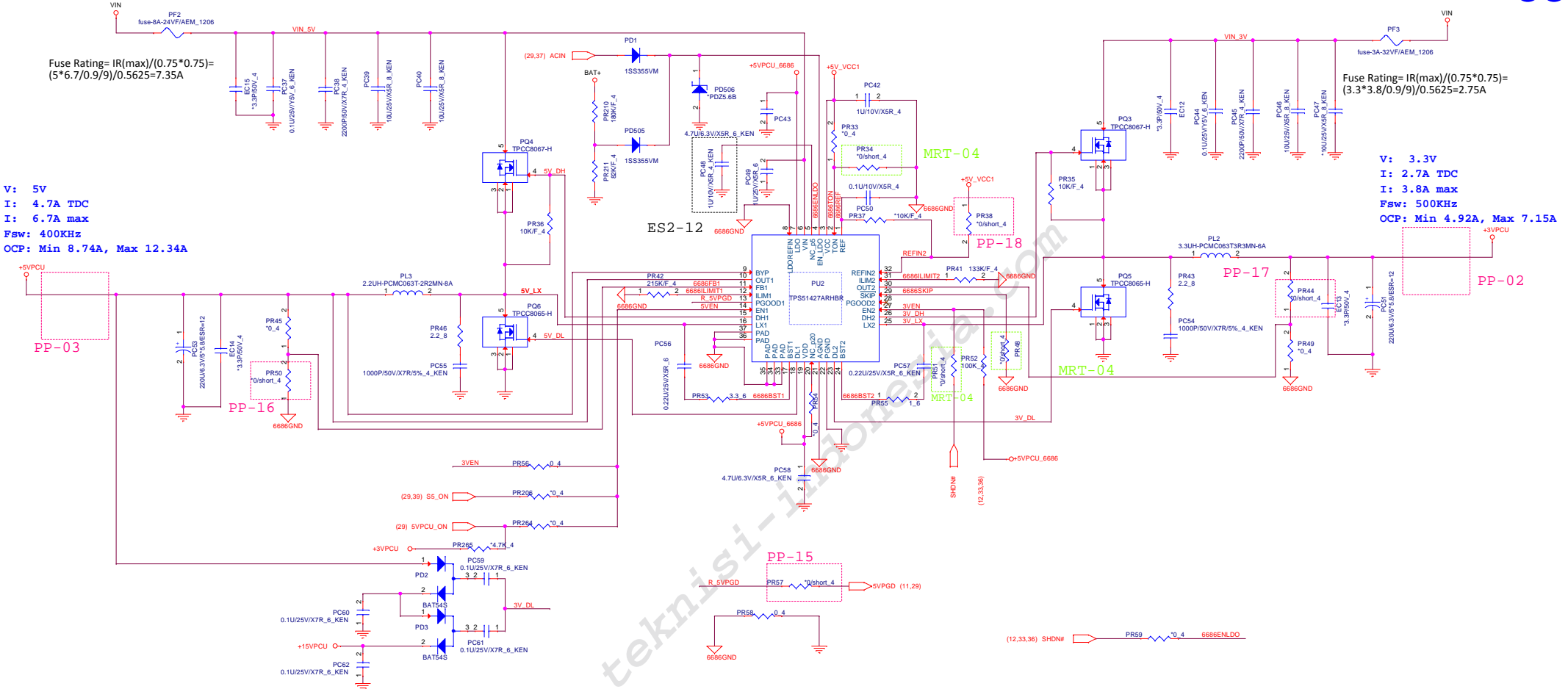


NUT





System +3VPCU & +5VPCU (TPS51427ARHBR)



Fuse Rating= $IR(max)/(0.75*0.75)=$
 $(5*6.7/0.9/9)/0.5625=7.35A$

Fuse Rating= $IR(max)/(0.75*0.75)=$
 $(3.3*3.8/0.9/9)/0.5625=2.75A$

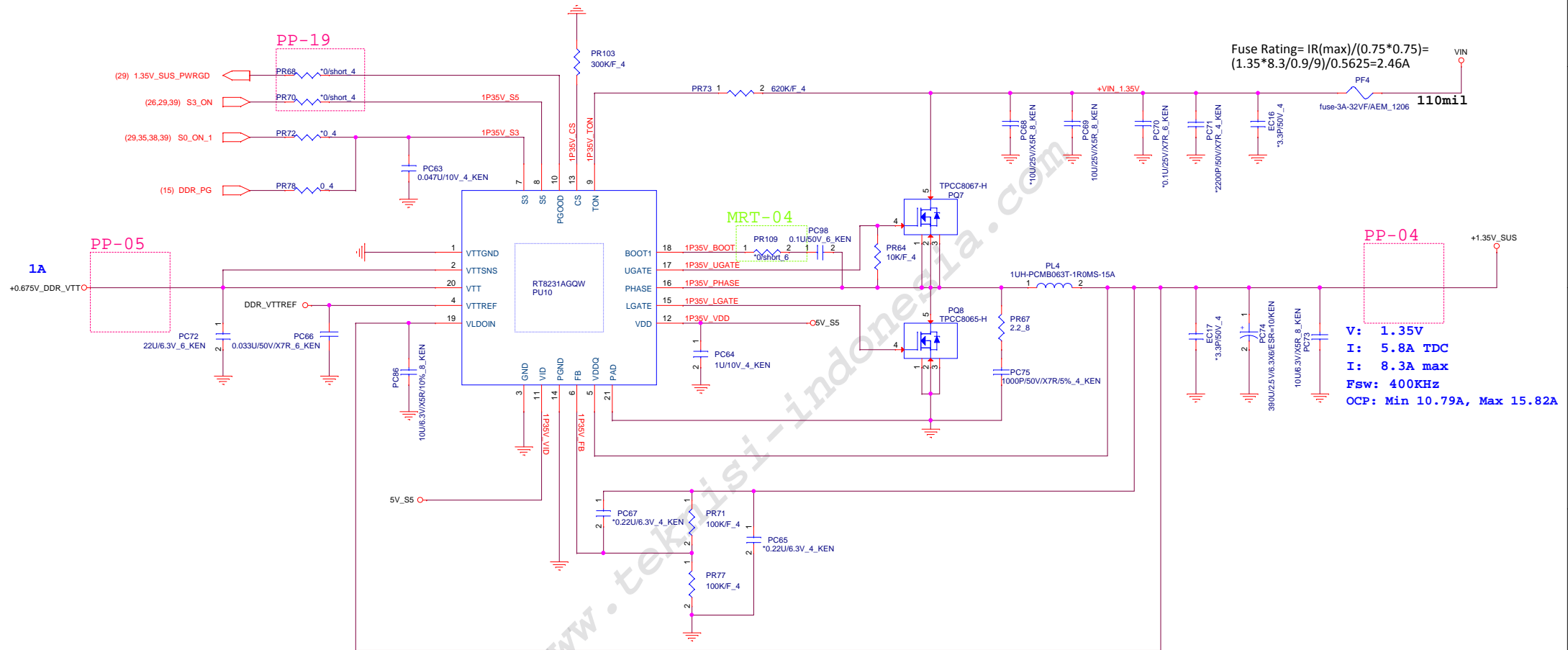
V: 5V
I: 4.7A TDC
I: 6.7A max
Fsw: 400KHz
OCP: Min 8.74A, Max 12.34A

V: 3.3V
I: 2.7A TDC
I: 3.8A max
Fsw: 500KHz
OCP: Min 4.92A, Max 7.15A

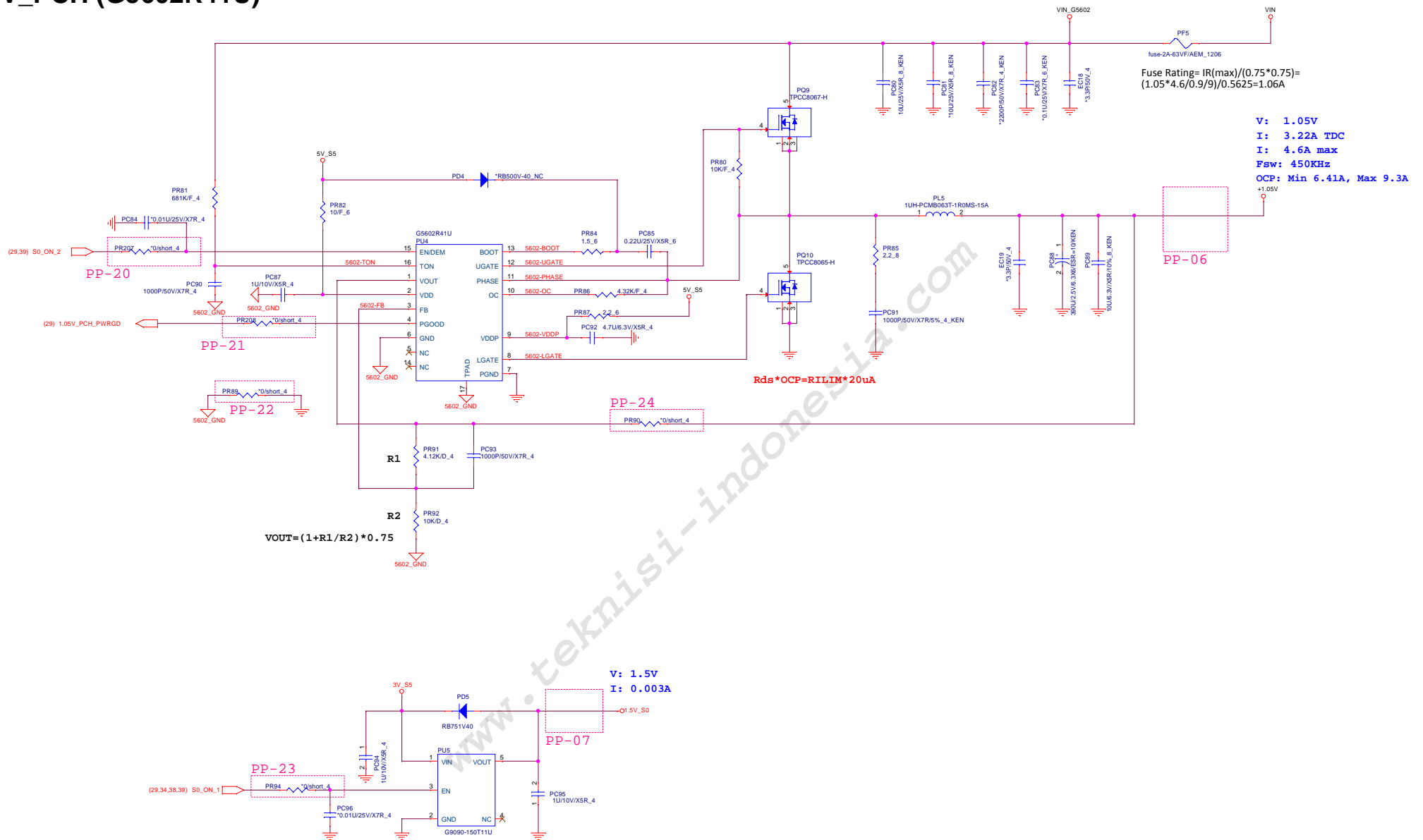
1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

DDR3 1.35VSUS &DDR_VTERM (RT8231AGQW)

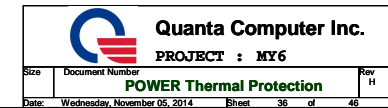
34



1.05V_PCH (G5602R41U)

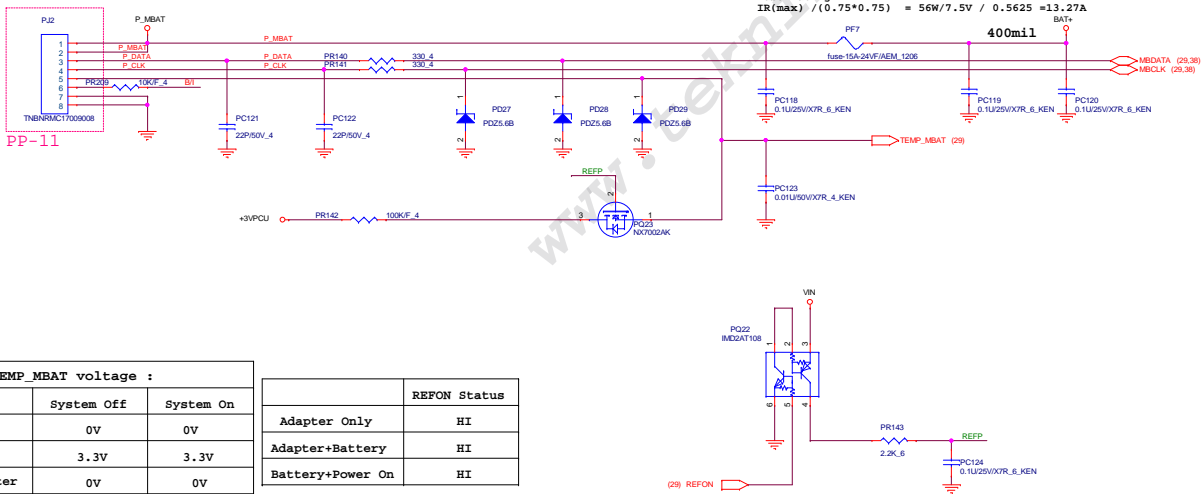
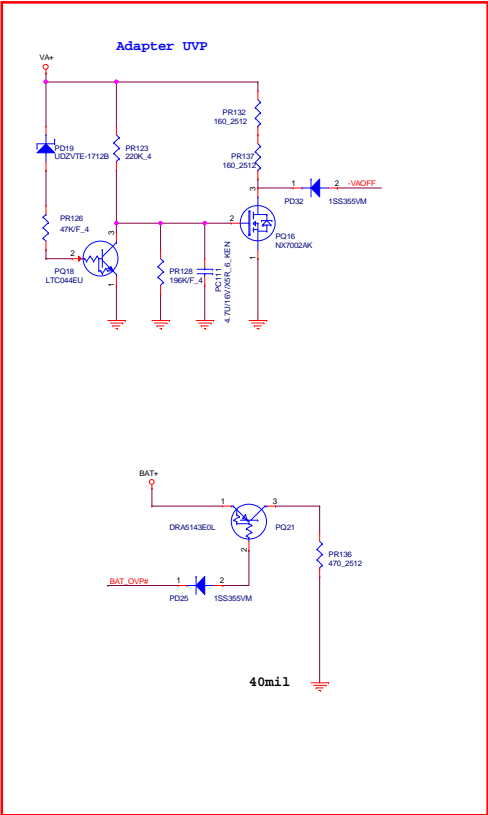
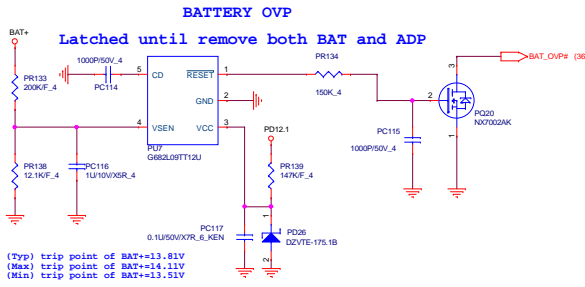
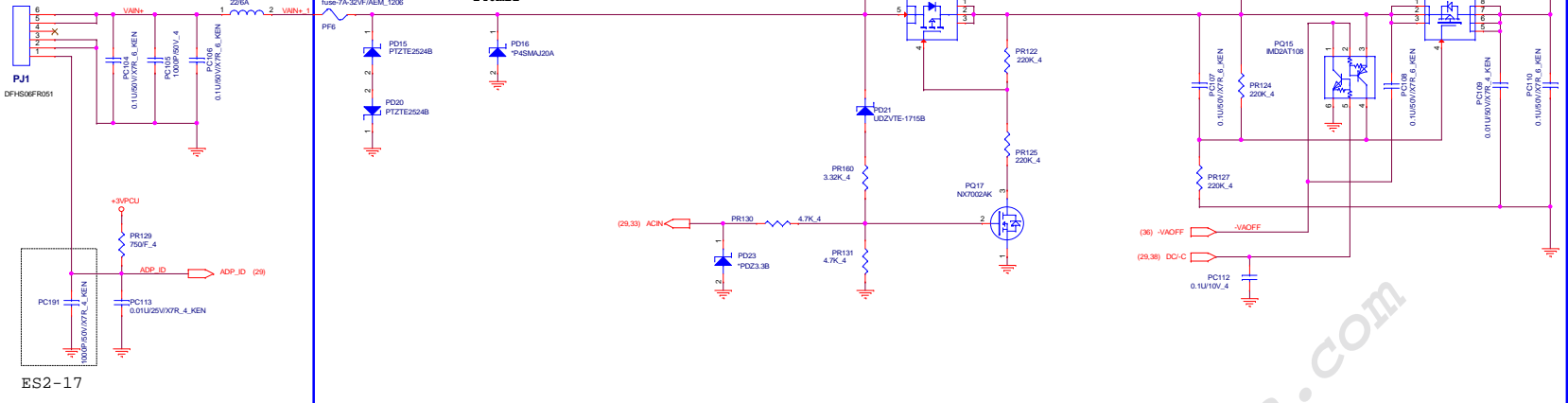


36



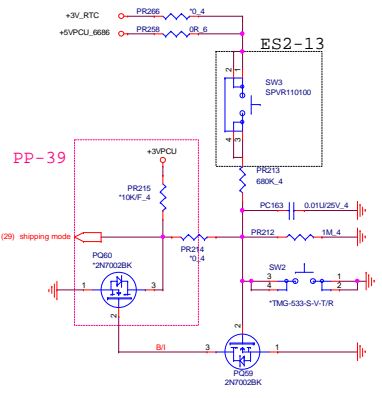
AC ADAPTOR IN CONN

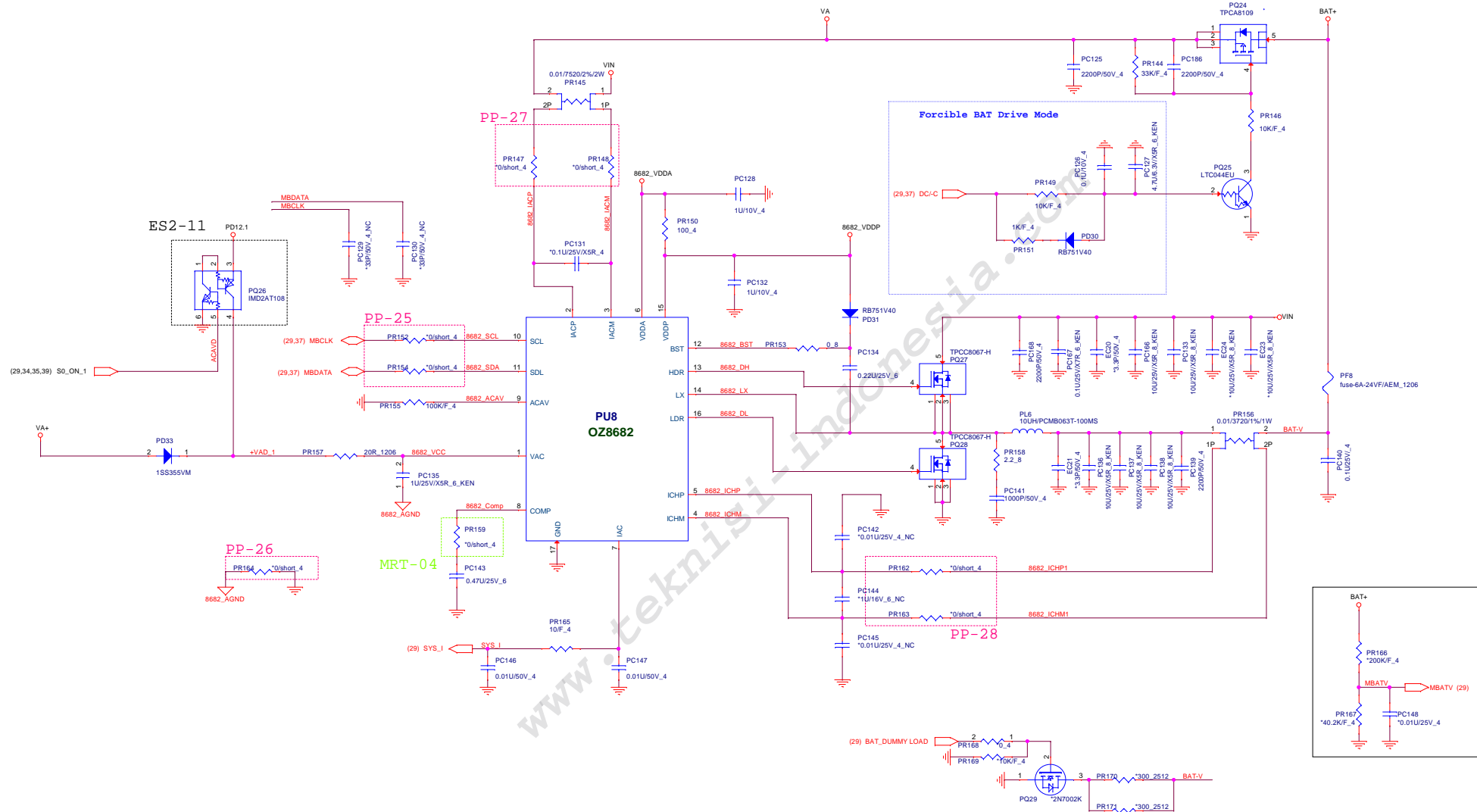
50320-0060N-001



TEMP_MBAT voltage :			REFON Status
	System Off	System On	
Battery	0V	0V	HI
Adapter	3.3V	3.3V	HI
Battery+Adapter	0V	0V	HI

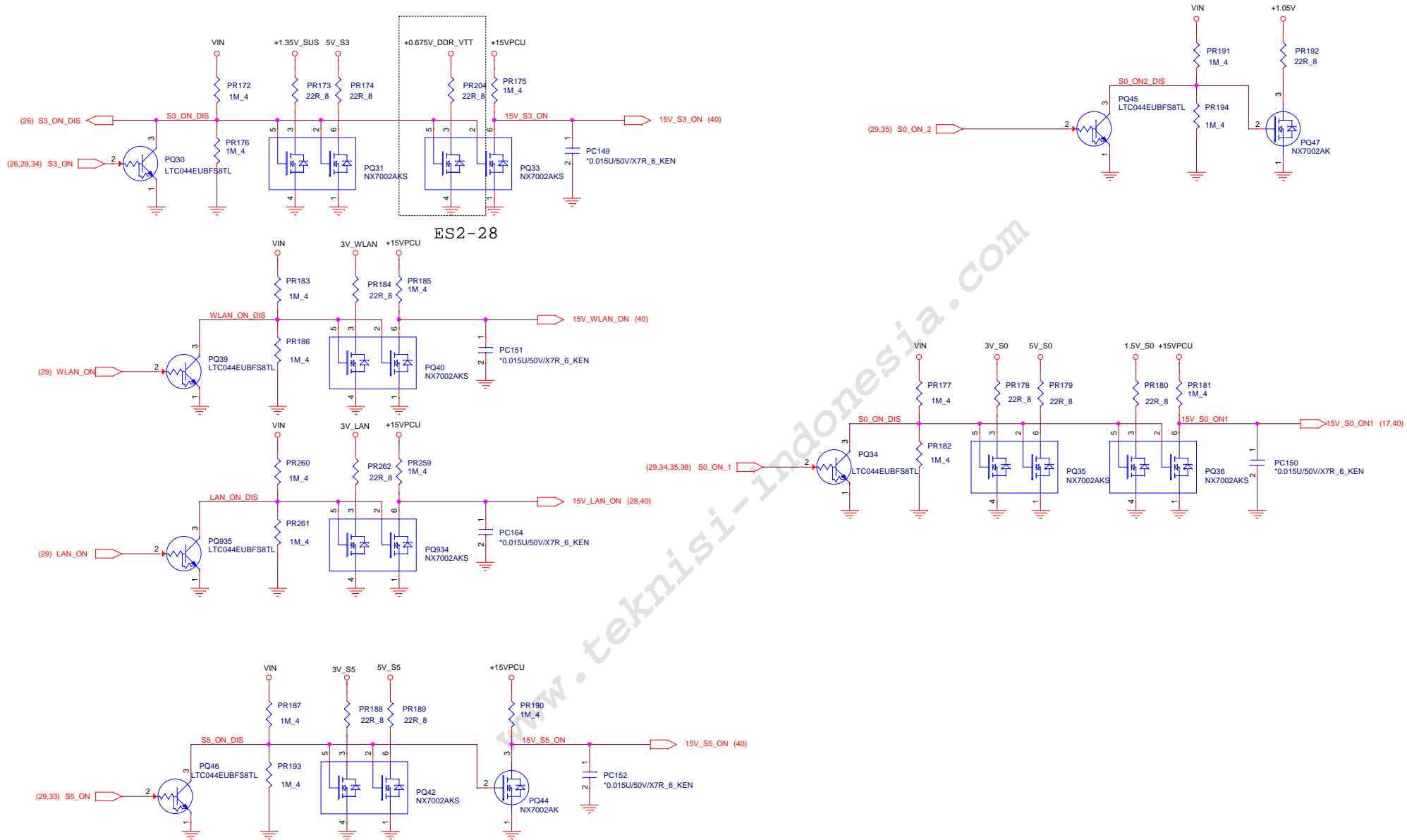
Shipping mode





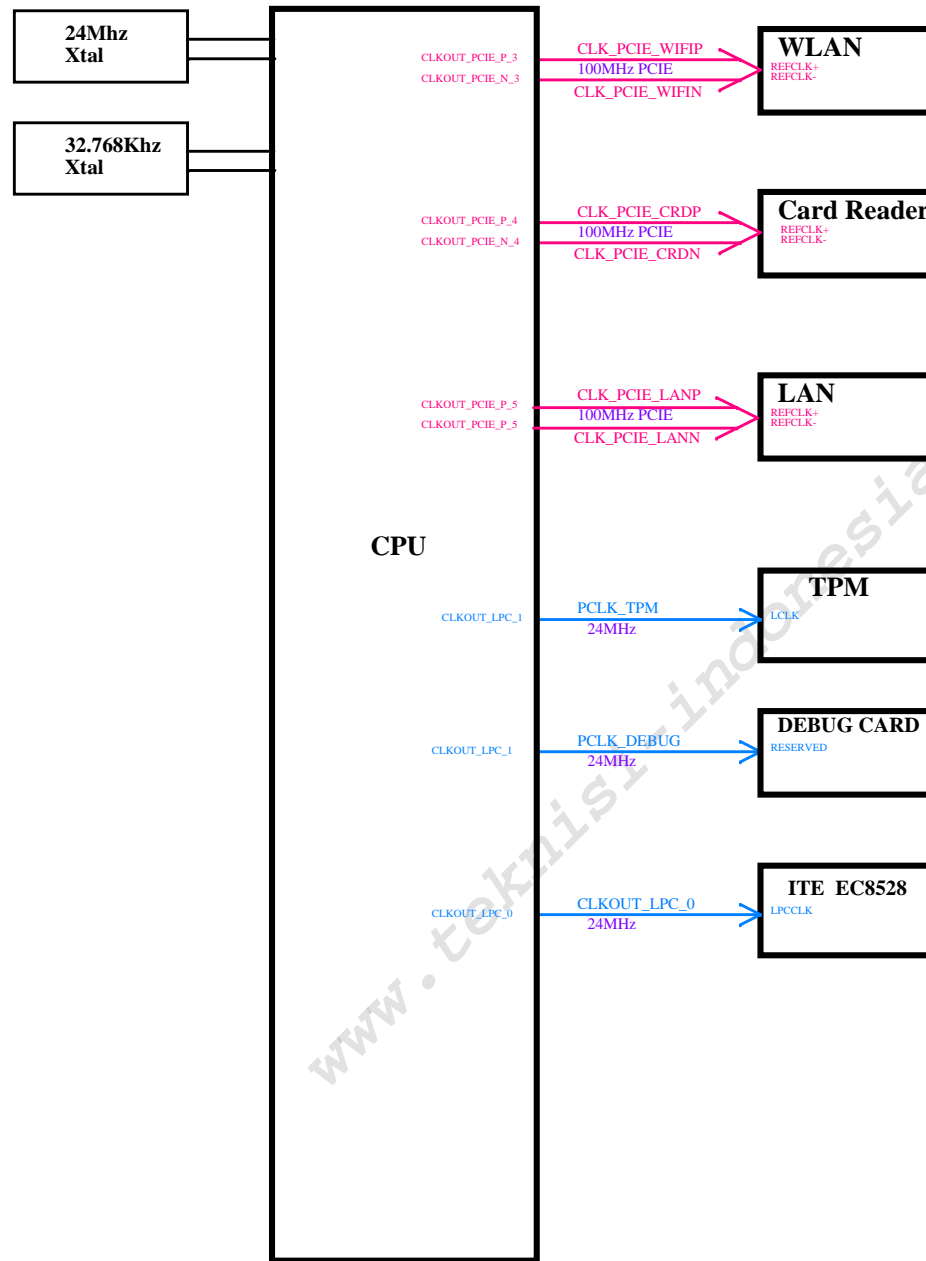
Power rail discharge

39



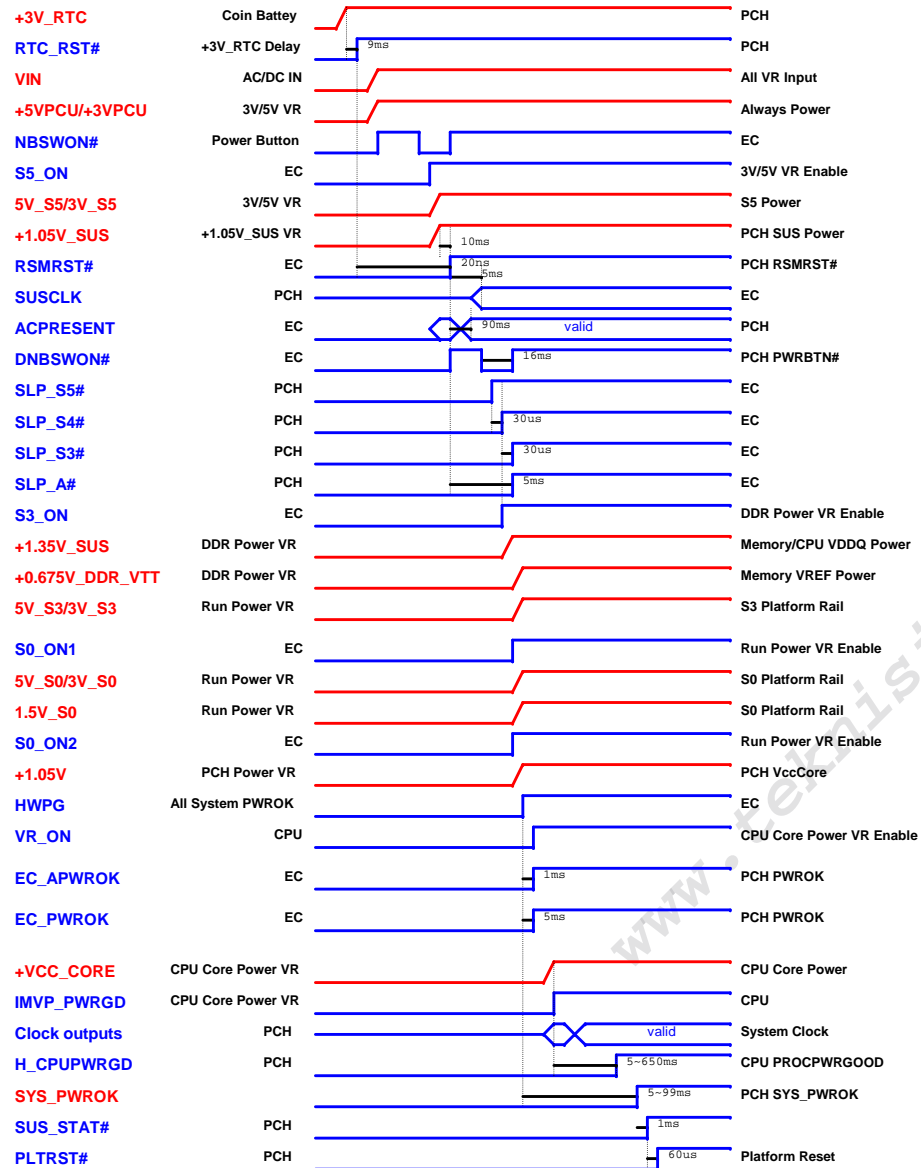
40

LAN_ON Load SW

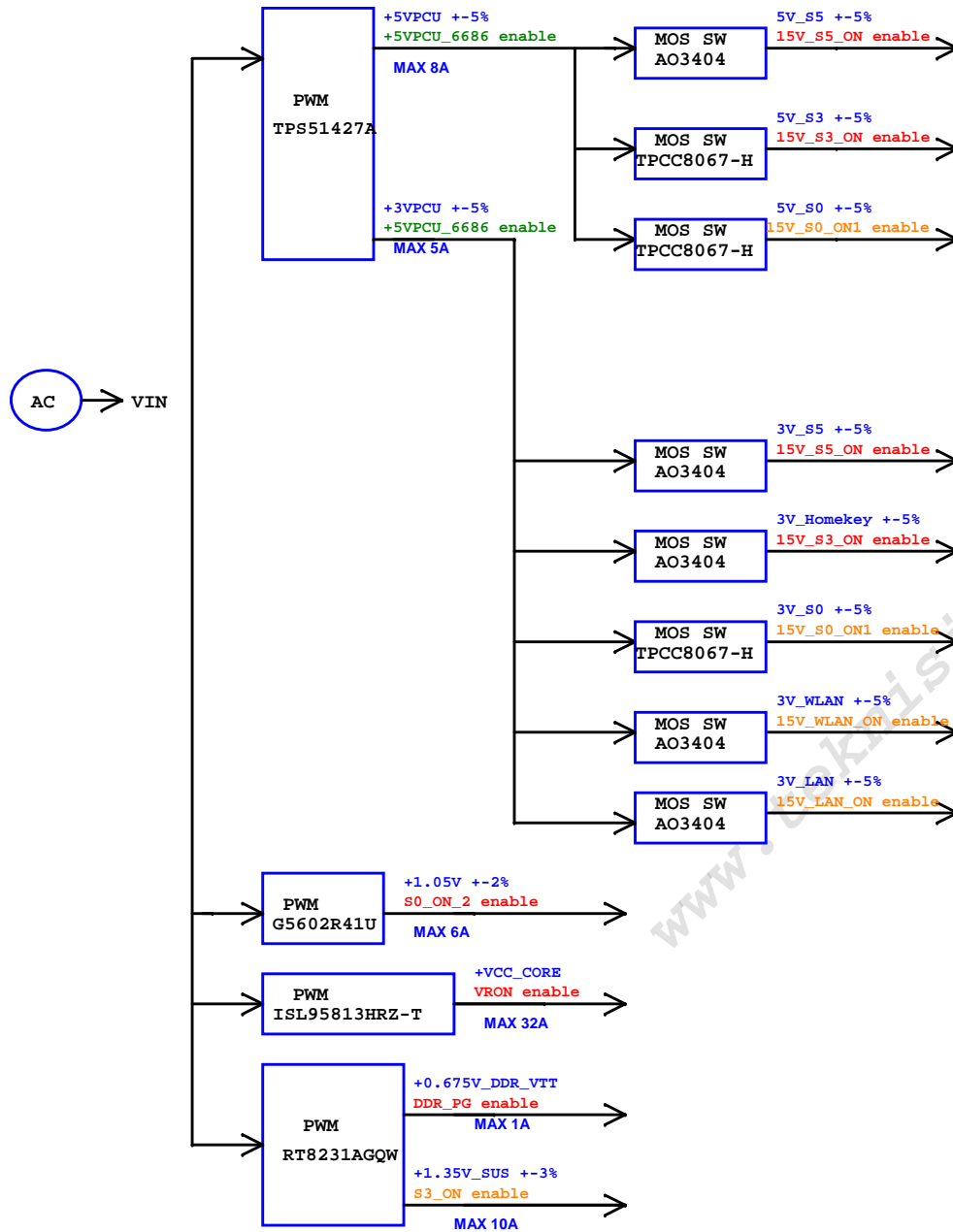


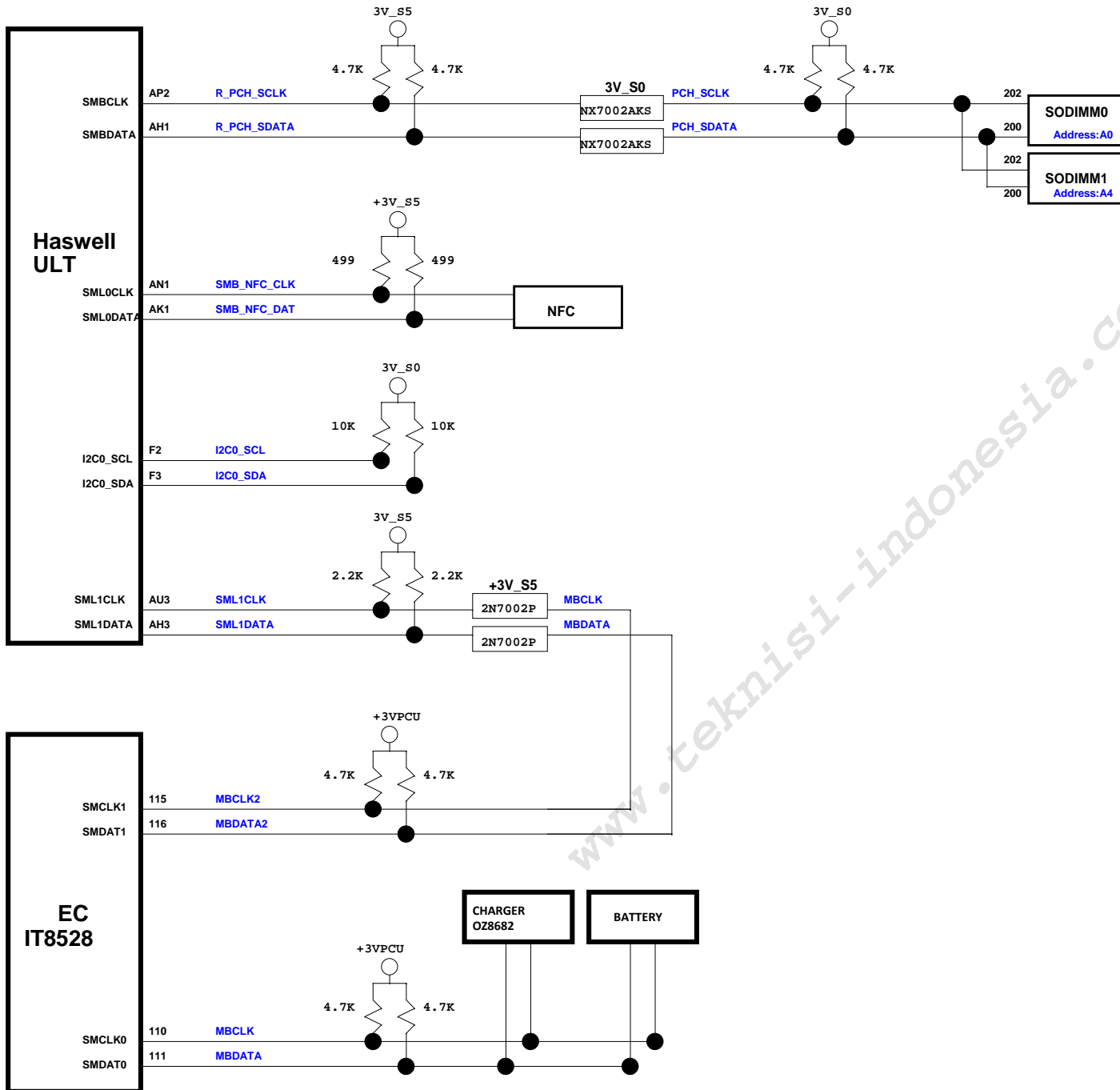
Power Sequence

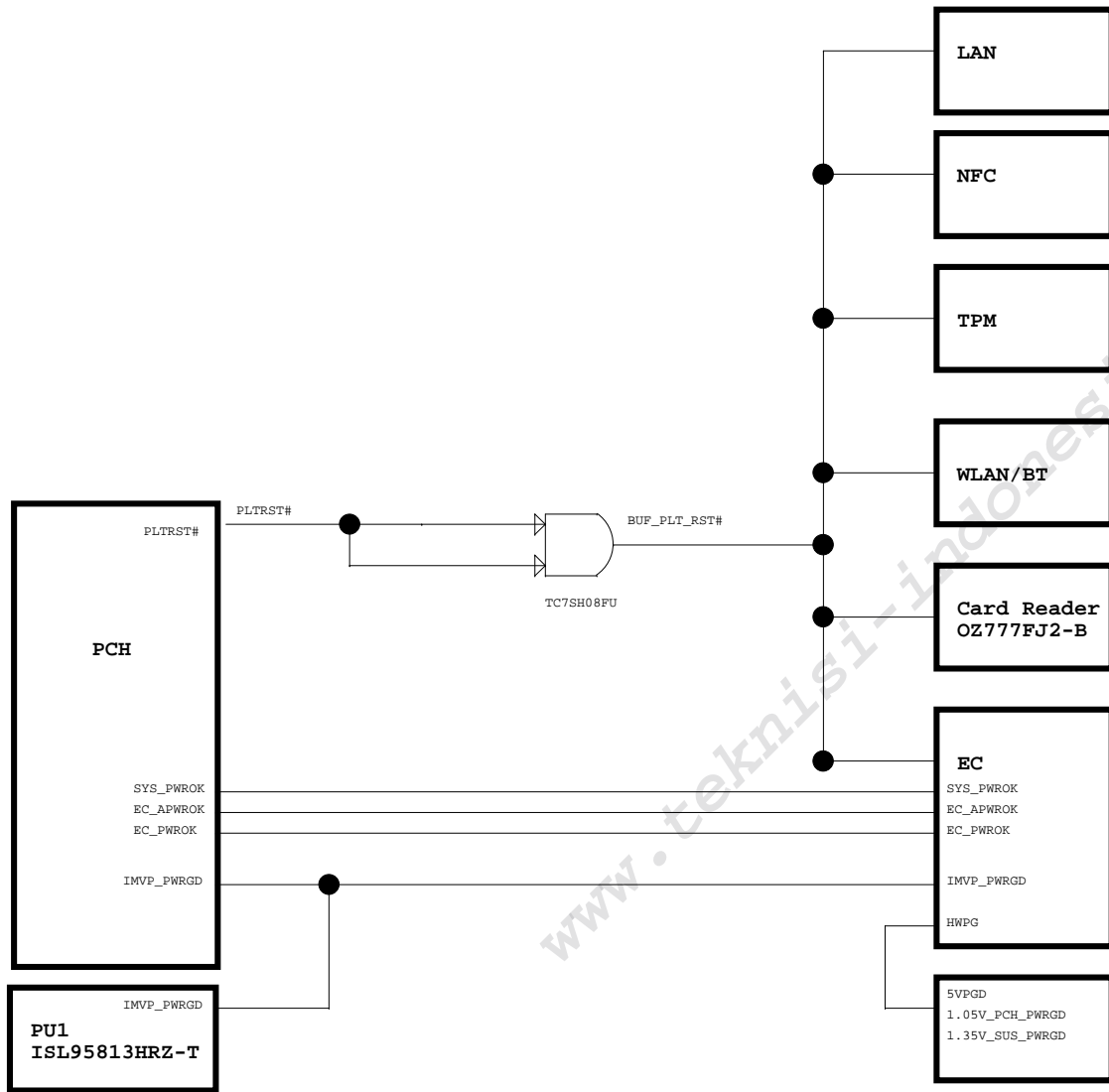
Timing Diagram for G3 to S0/M0 (non Deep Sx)



Power Tree Table







Model	REV	CHANGE LIST						
MY6 MB	ES2	ES2-01:Change USB3.0 CN11&CN13 P/N & footprint ES2-02:Change HDMI CN2 P/N & footprint ES2-03:Change Audio jack ACON1 P/N & footprint ES2-04:Add R594 for NFC_RSTW ES2-05:Change AC42,AC45,AC49,AC54 for EMI request ES2-06:Change SD card CN10 P/N & footprint ES2-07:Change R571,R572,R573 to 33 ohm for RST# undershoot & Overshoot ES2-08:Change PC165 to 2200p for 3V_LAN rise ES2-09:Change R158 to 2K for meet tCPU13 Sequencing ES2-10:Change NFC CON7 P/N & footprint ES2-11:Change PQ26 footprint ES2-12:Change +3VPCU & +5VPCU PC48 for 3.3V LDO stable ES2-13:Change SW3 for NEC request ES2-14:Add AR64 for EMI request ES2-15:Add AR20 for EMI request ES2-16:Add 3V_Homekey circuit for touch panel ES2-17:Add PC191 for EMI request ES2-18:Change RJ45 CON1 P/N & footprint ES2-19:Add detect RTC voltage circuit ES2-20:PC153 change to 0.01u for WLAN inrush ES2-21:R456 and R488 modification for IPOD charge issue ES2-22:D2 type change to RB500V for 3V_PCU leakage to RTC_3V ES2-23:R250&R251 change to NO STUFF for display flash issue ES2-24:Change eDP CN20 P/N & footprint ES2-25:Change BOARD ID to ES2 ES2-26:Add C571 in detect RTC voltage circuit ES2-27:Add EC cr1 HPD circuit ES2-28:Add +0.675V_DDR_VTT discharge circuit						
	PP	PP-01:Add C518 for EMI request PP-02>Delete PR39 for PP stage PP-03>Delete PR40 for PP stage PP-04>Delete PR63 for PP stage PP-05>Delete PR62 for PP stage PP-06>Delete PR83 for PP stage PP-07>Delete PR93 for PP stage PP-08>Delete R364,R365,R366,R367,R288 0 ohm to short PAD. PP-09:Stuff R127/R129/R132 for PP stage Board ID PP-10:Change RJ45 CON1 P/N & footprint PP-11:Change PJ2 P/N PP-12:Del R581 for NEC request PP-13>Delete PR4,PR5,PR6 0 ohm to short PAD. PP-14>Delete PR29,PR32 0 ohm to short PAD. PP-15>Delete PR57 0 ohm to short PAD. PP-16>Delete PR50 0 ohm to short PAD. PP-17>Delete PR44 0 ohm to short PAD. PP-18>Delete PR38 0 ohm to short PAD. PP-19>Delete PR68,PR70 0 ohm to short PAD. PP-20>Delete PR207 0 ohm to short PAD. PP-21>Delete PR208 0 ohm to short PAD. PP-22>Delete PR89 0 ohm to short PAD. PP-23>Delete PR94 0 ohm to short PAD. PP-24>Delete PR90 0 ohm to short PAD. PP-25>Delete PR152,PR154 0 ohm to short PAD. PP-26>Delete PR164 0 ohm to short PAD. PP-27>Delete PR147,PR148 0 ohm to short PAD. PP-28>Delete PR162,PR163 0 ohm to short PAD. PP-29>Delete PR196 0 ohm to short PAD. PP-30>Delete PR203 0 ohm to short PAD. PP-31>Delete PR197 0 ohm to short PAD. PP-32>Delete PR199 0 ohm to short PAD. PP-33>Delete PR198 0 ohm to short PAD. PP-34>Delete PR200 0 ohm to short PAD. PP-35>Delete PR195 0 ohm to short PAD. PP-36>Delete PR263 0 ohm to short PAD. PP-37>Delete PR10 0 ohm to short PAD. PP-38>Delete AR17,AR18,AR19,AR20,AR64 0 ohm to short PAD. PP-39:Add PR215 & PQ60 for charger LED on when SW3 open						
	MRT	MRT-01:Reserve EC CLR_CMOS circuit MRT-02:Stuff R131,Del R132 for MRT stage Board ID MRT-03>Delete AR14,AR27,R134,R139,R141,R234,R453,R452,R451,R450,R286 0 ohm to short PAD. MRT-04>Delete PR15,PR34,PR48,PR51,PR159,PR16,PR109 0 ohm to short PAD. MRT-05:Change Touch Power 5V_S3 to 5V_S0,Del F21 Add F24 0.5A.						
	DOC NO.		PROJECT MODEL :	MY6	APPROVED BY:		DATE:	2014/03/15
		PART NUMBER:		DRAWING BY:		REVISION:	1A	